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A 201A DATA COMMUNICATION ADAPTER FOR THE PDP-8:

Preliminary Engineering Design Report

David E. Wood

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A 201A DATA COMMUNICATION ADAPTOR FOR THE PDP-8: PRELIMINARY ENGINEERING DESIGN REPORT

David E. Wood

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A 201A DATA COMMUNICATION ADAPTOR FOR THE PDP-8: PRELIMINARY ENGINEERING DESIGN REPORT

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INTRODUCTION

This report discusses the design and use of equipment built for data communication to and from the PDP-8 through a 201A data set. The purpose of the data communication interface is to allow a PDP-8 to send and receive digital data through a 201A data set in a half-duplex mode. The 201A data set operates serially at a rate of 2000 bits per second, with the transmit clocks supplied by the data set. In the receive mode, the data set achieves bit synchronization, and provides a receive clocking signal to the interface. The interface provides the character synchronization at the start of a message and then transfers successive characters in parallel to the PDP-8. The interface stores and retrieves characters from the PDP-8 memory through the data-break facility, while achieving control communication with the PDP-8 through the interrupt and programmed data transfer modes.

This report will serve as a progress report for those interested in technical progress on the project, and as a rudimentary maintenance manual for those responsible for system maintenance in the future. Basic design objectives and decisions will be described first. A brief overall system description together with a sketch of a data format scheme and programming considerations will be followed by a detailed description of the interface logic.

DESIGN OBJECTIVES

In order to obtain a flexible interface the following design objectives were set forth:

1. Rigid interrupt discipline.
2. Minimal program interaction required during message transmission.
3. Variable character length and vertical parity calculation under program control.
4. Maximal interface status and control available upon request.
5. Hardware implementation of character synchronization using the ASCII SYN character.

In order to minimize the amount of code in an interrupt processor for the 201A communication interface, the interface was carefully designed to give interrupts <u>only</u> and <u>always</u> when a character was received or transmitted. The desire to give the maximum time between interrupts at the minimal hardware cost led to a decision to use core buffers in the PDP-8 through the use of the data-break facility. This decision was also made in light of the fact that several of these interfaces were to be used on the Data Concentrator. A separate design using a hardware buffer without using the data-break facility is shown in Appendix III.

The expected mode of operation of the interface utilizes an 8-bit character without vertical parity. Experimental evidence during the past year has indicated that vertical parity, at least on local hook-ups, is not needed. The decision to use an 8-bit character was strongly influenced by ASCII conventions and the fact that the central computing facility uses an 8-bit byte IBM/360 model 67 computer.

The interface depends on the PDP-8 only to the extent that characters must be removed or placed in the core buffers,

and the interrupt processed within a character time for error-free transmission. However, complete control and status presentation is available from the interface if desired, to the extent that the 201A data set will allow.

SYSTEM DESCRIPTION

The four sections of the equipment for one end of a data communication link are shown in Figure 1: the PDP-8, the PDP-8/201A line adaptor interface, the 201A line adaptor, and the 201A modem. The PDP-8 and the 201A modem will not be discussed here. This report is concerned with the design of the line adaptor and the line adaptor interface.

The distinction between the line adaptor and its interface is in some instances arbitrary. In general, however, the term line adaptor refers to that portion which is common to the three variations of the 201A data communications adaptor described in this report. The three variations which will be presented are: the basic PDP-8 adaptor, the PDP-8 adaptor which does not use data break, and the 201A line adaptors on the Data Concentrator. The PDP-8/201A line adaptor interface is hence that portion particular to the 201A communication link being considered.

Unless otherwise indicated, the basic PDP-8/201A line adaptor interface will be considered in the main body of the report. Detailed specifications of the 201A interfaces on the Data Concentrator and the 201A interface without data break are given in Appendices II and III respectively.

The subsystem designated by "201A Line Adaptor Control" in Figure 1 is specified in more detail in Figure 2. The basic component of the 201A line adaptor is the serial-deserializer register (SDR). This is a serial-in parallel-out or parallel-in serial-out shift register. It accepts and transmits to the 201A data set a serial data stream at 2000 bits/sec.

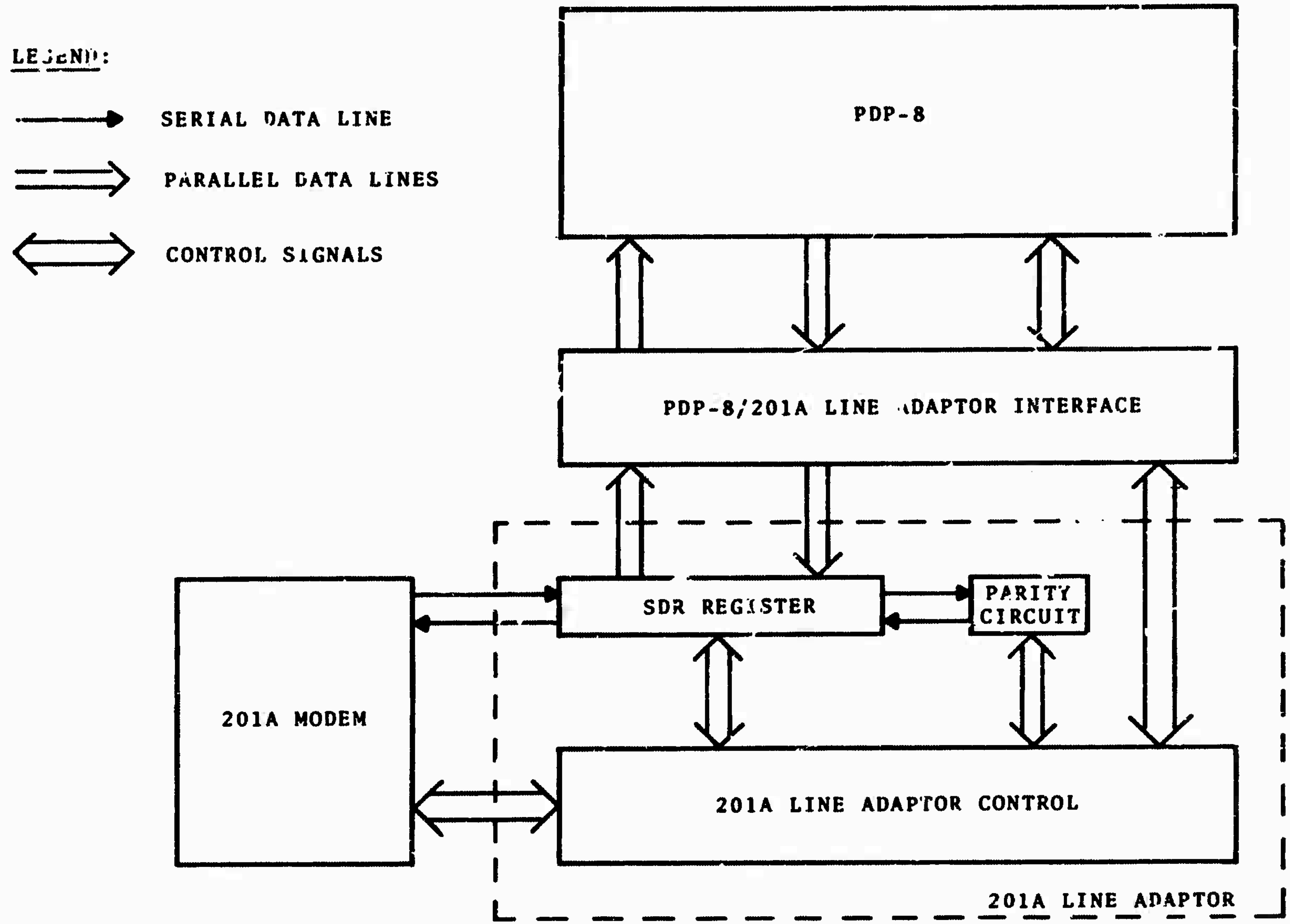

Figure 1. 201A COMMUNICATION LINK

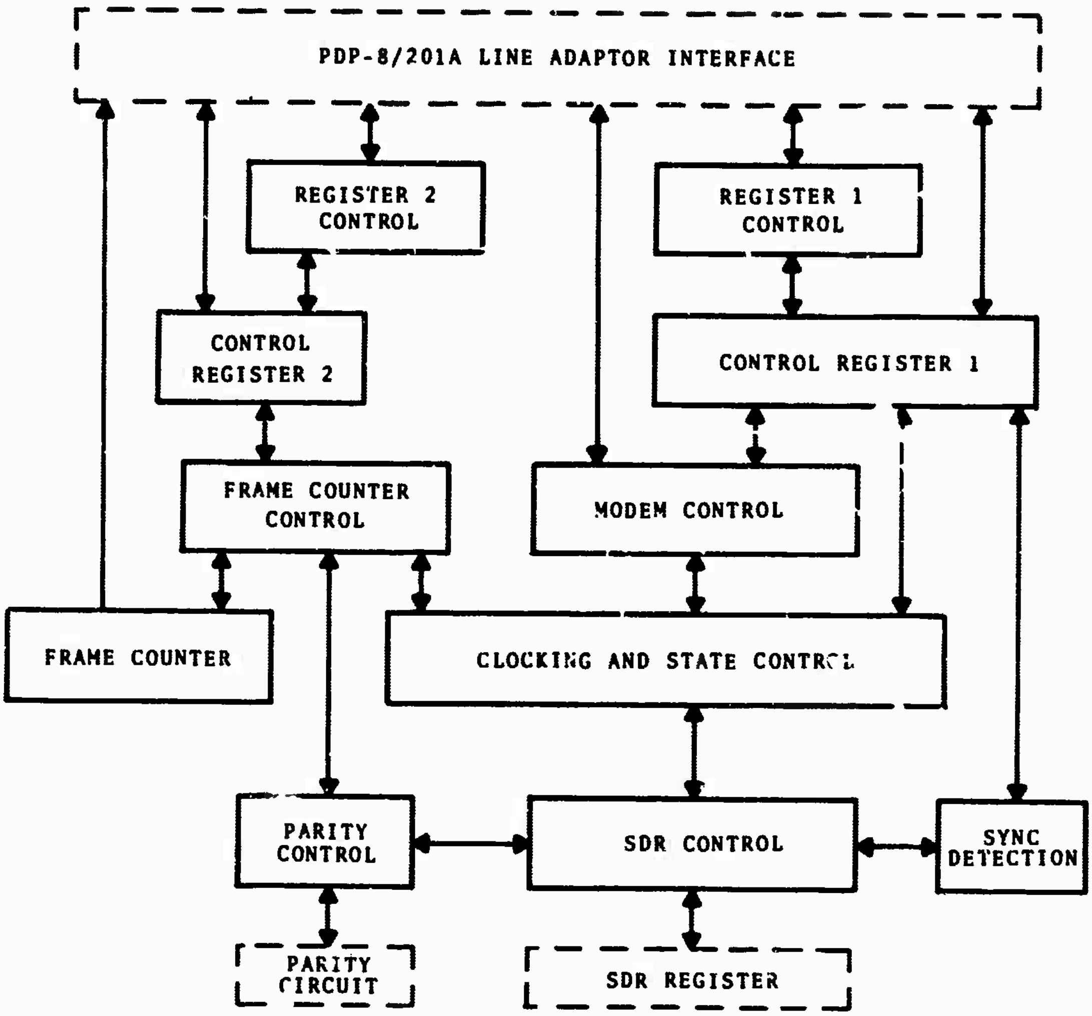

Figure 2. 201A LINE ADAPTOR CONTROL

On the other hand, it accepts from or transmits to the PDP-8 characters (usually 8 bits in length) in parallel. All clocking, with the exception of the data-break timing, is provided by the 201A data set.

The PDP-8 sees the 201A line adaptor (L.A.) as two control or status registers with all interaction being mediated through the manipulation of bits in these 2 registers. A detailed description of these registers as seen by the PDP-8 software is given in the next section. It is sufficient at this point to note that these registers, along with the frame counter, specify to the interface its state and hence the appropriate action to take at any given instant.

The frame counter is that counter in the line adaptor which determines when the correct number of bits have been shifted into or out of the SDR register. When the frame counter overflows, the character is data-breaked into core, in the case of a receive operation, or a new character is loaded into the SDR register from core in the case of a transmit operation. At the same time, an interrupt flag is set and the frame counter is reloaded. The L.A. then continues to assemble or dissassemble the next character while the proceeding interrupt is being processed by the PDP-8. This process is repeated over and over again for each character of the message. If, however, the interrupt flag has not been cleared when the next interrupt is generated, a Data Lost flag is set in additio as an error indication to the PDP-8.

When vertical parity calculation is enabled in the L.A., the frame size is assumed to include a parity bit as the high-order bit. The parity calculation is based on odd parity, and a parity error will cause only the Parity Error flag to be set, with no other abnormal action initiated by the L.A. The remaining function of the L.A. is to achieve character synchronization. This is accomplished by scanning the received data stream for a given bit pattern designated by SYN (026_8).

When this pattern is found, the interface is placed in what is called the text mode state, and the actions described above then take place. At the discretion of the PDP-8 software, the L.A. can be taken out of the text mode state, with the result that the scanning process will be resumed.

The control sequences to transmit and receive data will be described below. The remainder of the L.A. consists of buffers and gates which will be described in detail in the section on logic.

The PDP-8/201A line adaptor interface performs the logical and electrical function of mating the PDP-8 and the 201A line adaptor. This entails the control of the data-break operation between the 201A L.A. and the PDP-8, gating necessary for programmed data transfer, and the logic required for the interrupt control between the two devices. The details of these operations are presented in Appendices I, II, and III since they vary among the three systems.

PROGRAMMING AND CONTROL CONSIDERATIONS

The PDP-8/201A data communication interface in the case of a standard PDP-8 with single-cycle data-break capabilities is controlled by the resident PDP-8 program via three sets of IOT instructions. The device codes for these three sets of IOTs must be consecutive with the first one divisible by 4.* For example, 40, 41, and 42 are not used on most PDP-8 installations and satisfy the requirements. Furthermore, the hardware specifies (at the option of a given installation) two locations in core to be used as receive and transmit buffers. These locations must also be sequential with the convention that: receive $\equiv 0 \pmod 2$ and transmit $\equiv 1 \pmod 2$.

After the 201A L.A. transfers a word between the SDR register and the core buffer, the 201A L.A. will generate an interrupt. The first set of IOTs will service the interrupt

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* that is, the second octal digit is either a 0 or 4.

as follows:

Identify Transmit Interrupt (6xx1)

This micro-instruction causes a skip if an interrupt caused by a 201A transmit operation is pending.

Identify Receive Interrupt (6xx2)

This micro-instruction causes a skip if an interrupt caused by a 201A receive operation is pending.

Clear 201 Interrupts (6xx4)

This instruction will cause the 201A transmit and receive interrupt flags and the character service flag in the 201A status word to be cleared.

The 201A L.A. has two status or control words associated with it. Control Word 1 is serviced by the second set of IOTs and Control Word 2 by the third. (Figure 3 gives the bit assignment of these control words, and their interpretation is given below.) The IOTs for Control Words 1 and 2 behave identically.

Read (6xx1)

The contents of the specified control word is ORed into the AC.

Skip Under Mask (6xx2)

The PDP-8 will skip the next instruction if any position of the AC is a one and the corresponding position in the control word is a zero.

Invert Under Mask (6xx4)

This instruction inverts (complements) each bit of the control word for which there is a one in the AC.

CONTROL WORD 1:

AC POSITION	0	1	2	3	4	5	6	7	8	9	10	11
	INT FLAG	DATA LOST	PAR ERROR	REQ SEND	XMT REQ	CLR SEND	CHK PAR	TEXT	SET RDY	TERM RDY	RING	CAR DET

CONTROL WORD 2:

AC POSITION	8	9	10	11
	CFR(3)	CFR(2)	CFR(1)	CFR(0)

Figure 3. BIT ASSIGNMENT OF CONTROL WORDS

The first status register, called Control Word 1, is the basic 12-bit control register for the 201A L.A. It contains the necessary status information to control the 201A data set and L.A., and to determine its state. The second status register, Control Word 2, is a four-bit register which contains the modulo 16 complement of the character or frame size, not including vertical parity. When vertical parity is enabled, as noted above, the frame size includes a bit position for parity even though it is only detected and used by the hardware. For example, in normal operation, the character size is 8 bits with vertical parity checking and computation disabled; thus Control Word 2 in this instance would contain 10_8. The restrictions on the frame size from a hardware point of view are that it be greater than 2* and less than or equal to 12_{10}, including parity.

The following definitions give the name of each bit in Control Word 1 and its position relative to the AC along with the prescribed effect the software should have on each status bit. The operations available to the software (read, clear, and invert) are indicated in parentheses.

INT FLAG—Interrupt Flag (Clear) (AC0)

When receiving, indicates that a character has just been placed in the receive buffer. When transmitting, it indicates that a character has just been taken from the transmit buffer and will be transmitted. An interrupt will occur only and always in these cases.

DATA LOST—(Clear) (AC1)

Indicates that an interrupt has occurred when the INT flag is set. This should indicate, if interrupts are processed correctly, that overrun has occurred and hence a character has been lost (receive) or a duplicate character sent (transmit).

*Note: The SYN character is constrained to be 8 bits.

<u>PAR ERROR</u>—Vertical Parity Error (Clear) (AC2)

Indicates a vertical parity error has occurred on the present character received. This indication will occur only if bit AC6 is set (see description below).

<u>REQ SEND</u>—Request-to-Send (Read)(AC3)

This is a data set control signal which tells the data set to produce a carrier and begin transmitting when the clear-to-send signal comes on. This signal is generated and cleared via transmit request in a manner described below.

<u>XMT REQ</u>—Transmit Request (Invert) (AC4)

By setting this bit, the request-to-send bit is set if the 201A L.A. is not in the receive state. If the 201A L.A. is actively receiving, the receive operation is terminated at the next end-of-character indication and then the request-to-send signal is given. If the 201A L.A. is actively transmitting and XMT REQ is cleared, the 201A L.A. will go into the receive idle state at the next end-of-character indication, that is, waiting for the carrier to be detected from the other end of the line.

<u>CLR SEND</u>—Clear-to-Send (Read) (AC5)

Indicates that sufficient time has elapsed since the request-to-send indication was given and the line is now in a transmit ready state. This indication is <u>not</u> the data set clear-to-send signal, but an indication derived from the data set signal which guarantees proper operation of the interface.

<u>CHK PAR</u>—Check Vertical Parity (Invert) (AC6)

Indicates to the 201A L.A. that in the receive state vertical parity is to be checked, and in the transmit state vertical parity is to be computed and the correct bit appended to the character and transmitted. Vertical parity is always

computed in the 201A L.A., but no action is taken unless the CHK PAR bit is set. This continual computation allows the 201A L.A. to go from non-parity operations to parity operations within one character time.

TEXT—Text Mode (Invert) (AC7)

In the receive state, text mode indicates that character synchronization has been found. If the TEXT bit is cleared while in the receive state, this tells the interface to look for new character synchronization. While looking for character synchronization no interrupts will occur. The first interrupt will occur on the first character received following the establishment of character synchronization.

When in the transmit state, TEXT should normally not be altered. If the TEXT bit is cleared while transmitting, the interface is frozen until the TEXT bit is set again. This has the effect of transmitting continually the bit being presented to the line at the time the TEXT bit was cleared. During this time no interrupts will occur.

The 201A L.A. will always place the TEXT bit in the correct state. It should be changed under program control only if the actions described above are desired.

SET RDY—Set Ready (Read) (AC8)

Indicates that a call has been answered and that there is a data set in the data mode at the other end of the line. This indication drops when either party hangs up.

TERM RDY—Terminal Ready (Invert) (AC9)

Indicates to the data set that it should automatically answer a call.

RING—Ringing (Read) (AC10)

Indicates that the data set is being called. The indication follows the actual bell or ring signal to the hand set.

<u>CAR DET</u>—Carrier Detect (Read) (AC11)

Indicates that carrier is on the line. In most cases of normal operation when CLR SEND is on, it indicates that local carrier is present, and conversely when CLR SEND is off, that carrier is being received from the other end of the line.

Throughout the definitions above, reference was made to the transmit and receive states. These states are defined within the 201A L.A. as the logical conjunction of certain signals. That is, the 201A L.A. is in the <u>transmit state</u> if and only if <u>all</u> the following signals are present:

a. REQ SEND
b. CLR SEND
c. SET RDY
d. TERM RDY
e. CAR DET

The 201A L.A. is in the <u>receive state</u> if and only if <u>all</u> the following conditions are true:

a. REQ SEND is <u>not</u> present
b. CLR SEND is <u>not</u> present
c. SET RDY is present
d. CAR DET is present

The 201A L.A. is in the <u>receive-idle</u> state if and only if <u>all</u> the following conditions are true.

a. REQ SEND is <u>not</u> present
b. CLR SEND is <u>not</u> present
c. SET RDY is present.

A DATA FORMAT SCHEME

For the sake of completeness a brief sketch and discussion of a message format scheme is presented. The only portion of this scheme which is affected by the hardware is the actual SYN character. This particular scheme is presented for exposition purposes only and is not intended to represent the existing 201 software support.

An <u>inbound message</u> has the following format:

<Sync Characters><Text Characters><Terminating Character><Two Block Check Characters>.

These characters are defined as follows:

TABLE I

CONTROL-CHARACTER DEFINITIONS

ASCII NAME	OCTAL	HEX	FUNCTION
ETX	003	03	End of Text
EOT	004	04	End of Transmission
ENQ	005	05	Enquiry
ACK	006	06	Positive Acknowledgment
NAK	025	15	Negative Acknowledgment
SYN	026	16	Synchronous Idle
ETB	027	17	End of Text Block
EOM	031	19	End of Message
PAD	377	FF	Pad for Line Turnaround

A <u>Sync Character</u> is the ASCII SYN character. A minimum of four sync characters will be required to guarantee proper character synchronization by the software. In the case of long distance operation where there is echo suppression on the telephone line a sufficient number of PAD characters must precede the SYN characters to allow the line to settle down.

A Text Character may be any combination of eight bits which is not identical to a terminating character. The positive acknowledgment character, ACK, and the negative acknowledgment character, NAK, are considered message characters for transmission purposes. Likewise SYN is a message character which when received is deleted from the message. The message may be the empty string, that is, no text characters.

A Terminating Character is any member of the following set of characters:

{ETX,ETB,EOT,EOM,ENQ} .

Each of these terminating characters will have the effect of terminating the present message along with other logical implications to the software.

The Block Check Characters are longitudinal parity check characters treated as a code word in a cyclic code whose generating polynomial is

$$X^{16} + X^{15} + X^{2} + 1 .$$

Two block check characters must accompany every message.

This format is used in a store and forward mode; that is, the PDP-8 receiving a message across a 201A data communication link will store the incoming message. Concurrently it will forward that message at a rate that the interrupt processing will bear, calculating the cyclic checksum as it proceeds. In general, when the terminating character is finally encountered in this forwarding operation, the two checksums (the one actually received and the one computed)are compared. If the two match, a positive acknowledgment ACK is returned to the sender. If a discrepancy exists, an NAK or negative acknowledgment is returned. The software determines what to do in these cases, and this problem will not be discussed here.

An outbound message has the same format as an inbound message with the addition of at least one PAD character appended to the end of the message to allow for proper "flushing" of the communication link. The PAD characters are always ignored in this context.

A graphical presentation of a message exchange as viewed from the PDP-8 is shown in Figure 4. For exposition purposes the handshake message has the form:

(SYN1)(SYN2)(TEXT CHAR)(ETX)(BCC1)(BCC2)(PAD1)(PAD2) ,

with the acknowledgment taking the form

(SYN1)(SYN2)(ACK)(ETX)(BCC1)(BCC2)(PAD1)(PAD2) .

In Figure 4, the control status is affected either by the program (P.S.-Program Set, P.C.-Program Clear) or by the data set or interface (D.S.-Modem Set, D.C.-Modem Clear).

DETAILED LINE ADAPTOR LOGIC

This section will present in detail the logical design of the 201A line adaptor. The logic diagram follow standard Digital Equipment Corporation conventions. A working knowledge of D.E.C.'s R and W series logic is assumed throughout this section. The remainder of the logic for the 201A Interface is given in Appendices I, II, and III for each particular version of the interface. For completeness, both the module position and pin assignment for each circuit is indicated. All circuits within this section are in the same D.E.C. 1943 wire-wrap panel. The detailed module utilization is presented with the particular interface in the Appendices. In order to allow for multiple adaptors, as used on the Data Concentrator, the common signal names are prefixed with a # sign. In a single adaptor configuration the # sign is just part of the signal name. The logic will be presented as much as possible within the framework of Figure 2.

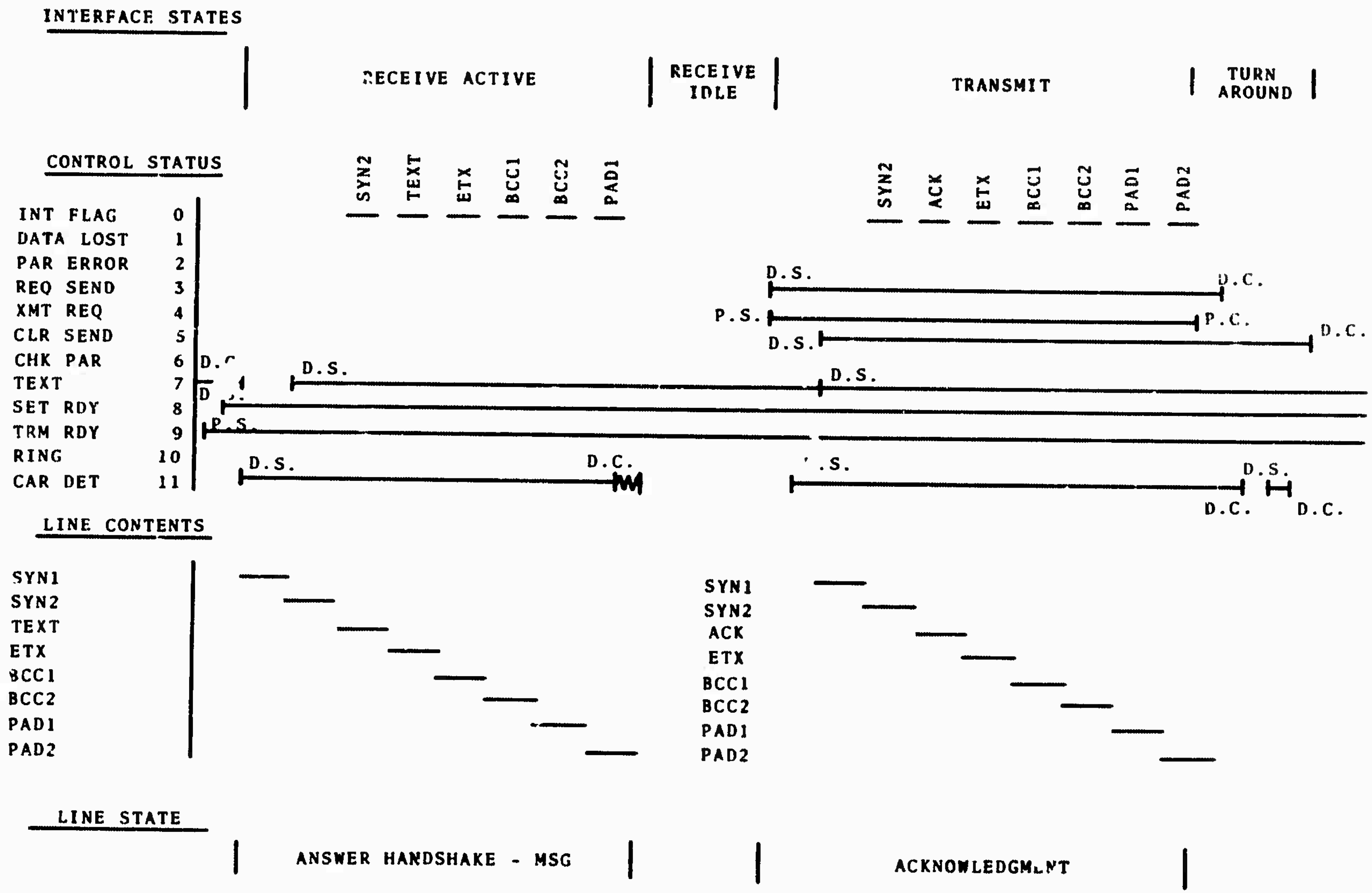

Figure 4. Graphical Presentation of a Message Exchange Viewed from the PDP-8.

Serial-Deserializer Register (Diagram 1)

This is a 12-bit register with high-order position #SR00 and low-order bit #SR11. Serial data are shifted into #SR00 in the receive state from the data set on the clock signal #SHIFT. They are shifted out of #SR11 in the transmit state into a line buffer #SDBF. Characters are strobed into the SDR register in a data-break operation from the buffered memory buffer on the #MBSR signal. This character transfer is simulated in the case of an interface not using data break, and those details are treated in Appendix III. The operation of character transfer to the PDP-8 is treated in the Appendices.

Clock Gating (Diagram 2)

The 201A data set provides two clock signals, #SCRB (receive clock) and #SCTB (transmit clock). The #SCTB clock is always available and is used within the data set for internal control timing. The #SCRB clock is derived from the received data stream and is provided to sample the received data line (#RDB). The interface selects the correct clock on the basis of its state (transmit/receive).

SDR Pulse Gating (Diagram 3)

The control of the SDR register is primarily achieved through the four pulse amplifiers (Diagram 3). To keep all transitions occurring synchronously with the #CLOCK signal it is necessary to separate the clearing of #SR00 from the remainder of the register. By the use of the #FR3+ signal, the register is cleared at the end of a transmitted character before the next character is loaded. It is cleared at the end of a data-break operation in the receive state via #BRKDN; and all but #SR00 is cleared when character synchronization is found in the receive state. In this last case, while the remainder of the register is cleared the first bit is read in from the line. #MBSR loads ones into the register during a data break in the transmit state.

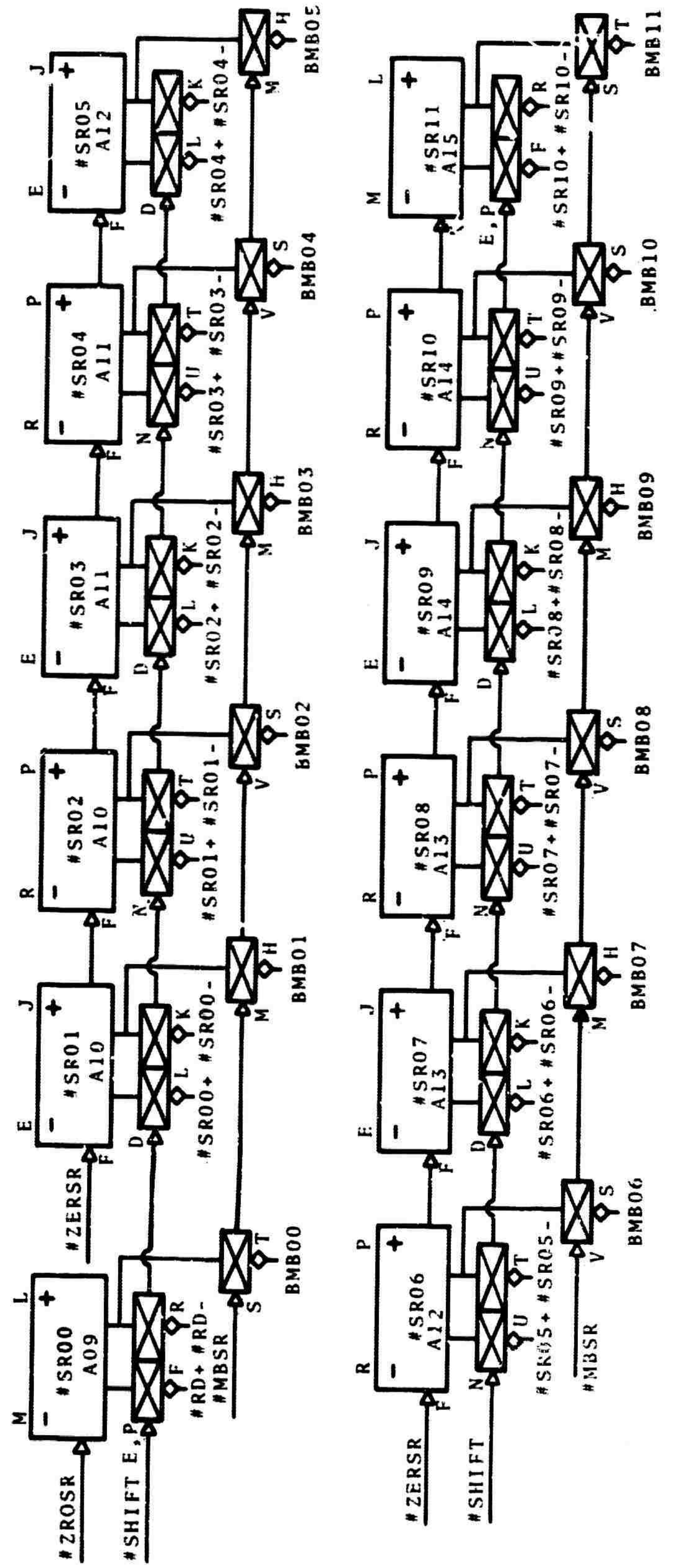

Diagram 1. SDR REGISTER

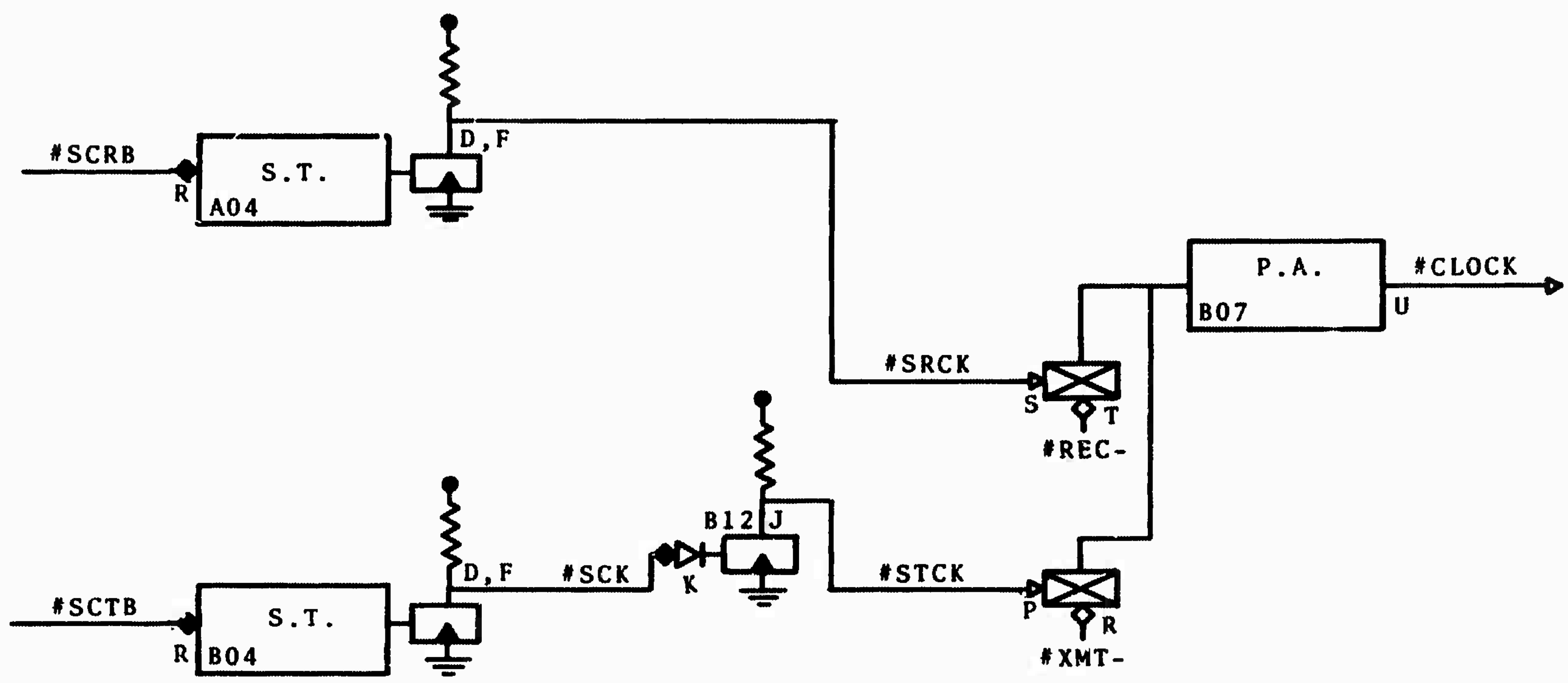

Diagram 2. CLOCK GATING

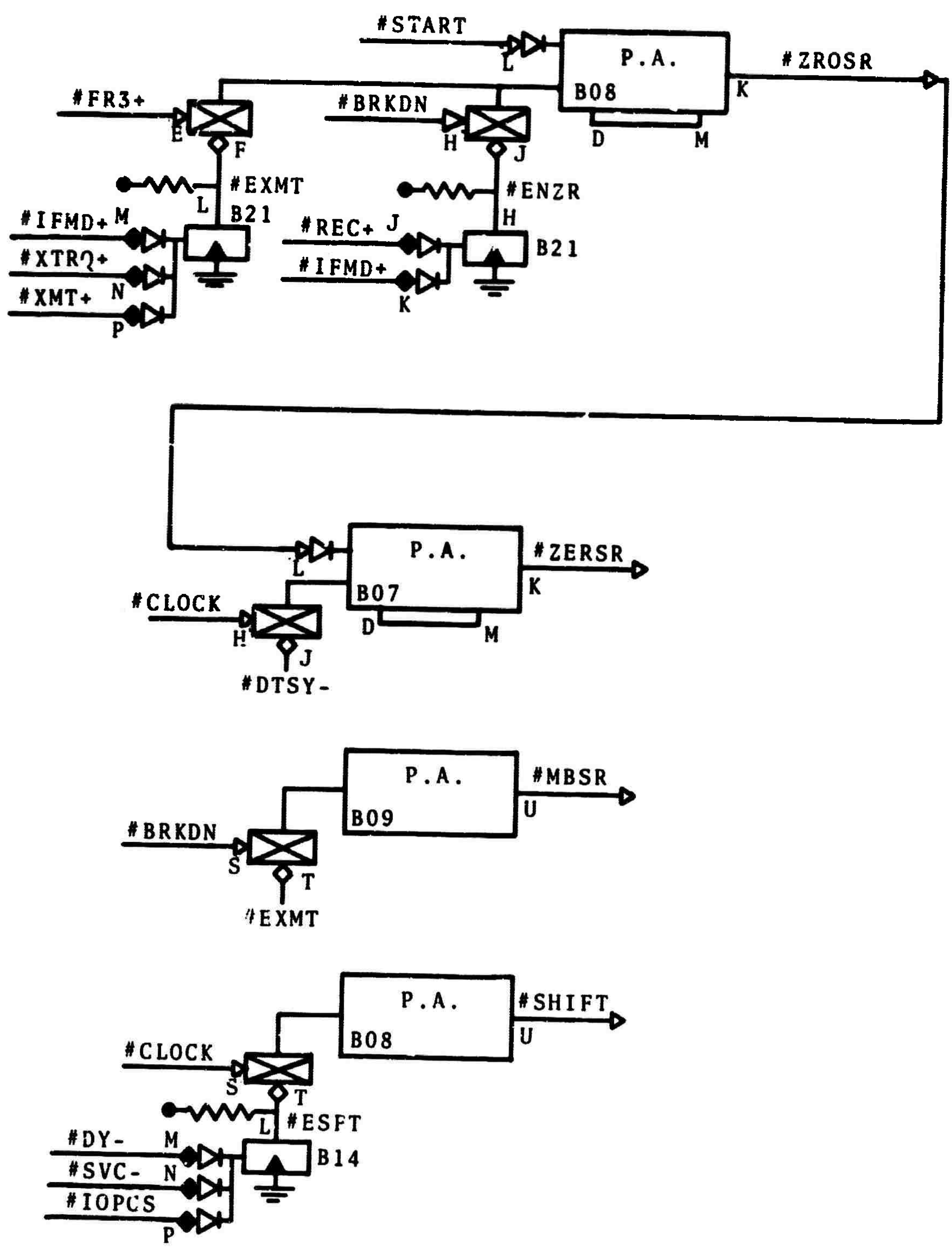

Diagram 3. SDR PULSE GATING

Data Set Signals (Diagram 4)

Diagram 4 shows the correspondence between the 201 data set connector and signal designations of the 201A L.A.

SDR Serial Input/Output Gating (Diagram 5)

The serial input signal #RDB from the 201A data set is converted to standard D.E.C. levels (-3v, 0v) from E.I.A. standard levels (+6v, -6v) (Electronic Industries Association Standard R S 232: Interconnection of Data Terminal Equipment with a Communications Channel). When not in the receive state, the input to the SDR register is conditioned (#RD+) to shift a zero into the SDR register. The #LINE flip-flop determines whether the output from the SDR register buffered via #SDBF or a parity bit (#PTBF) is placed on the transmit data line (#SDB). When the L.A. is in the receive state, zeros are always placed on the #SDB line to minimize possible cross-talk.

Transmit/Receive State Gating (Diagram 6)

The XMT/REC status of the interface is specified by the two flip-flops #XMT and #REC. The definition of these states has been defined above, however, it is important to note that the state changes are synchronized to the clock. The #RSYN latch is used to prevent the loss of the last receive interrupt.

Control Register 2 (Diagram 7)

The second control word as defined above contains the modulo 16 complement of the current character length. This value is referred to throughout the interface as the frame size and is stored in the register #CFR0-#CFR3. The register is loaded via IOT commands described above from the PDP-8 AC, and read into the PDP-8 on an extension to the AC called the EAC. The details of the EAC buss are described in Appendix I.

DIAGRAM 4

DATA SET/INTERFACE CABLE ASSIGNMENT

Interface Signal Name	Data Set Connector (CINCH DB-25-P PLUG)		Signal Name	Interface Connector (W021MJ*)
	1	AA	Protective Ground	C
	7	AB	Signal Ground	C
#SDB	2	BA	Transmit Data	D
#RDB	3	BB	Receive Data	E
#RSB	4	CA	Request to Send	F
#CSDB	5	CB	Clear to Send	H
#SRDB	6	CC	Set to Ready	J
#TRDYB	20	CD	Terminal Ready	K
#RINGB	22	CE	Ring	L
#CDETB	8	CF	Carrier Detect	M
#SCTEB	24	DA	Terminal Transmit Clock	N
#SCTB	15	DB	Set Transmit Clock	P
#SCRB	17	DD	Set Receive Clock	R

* Special module with all pins available and ground connections for shielding.

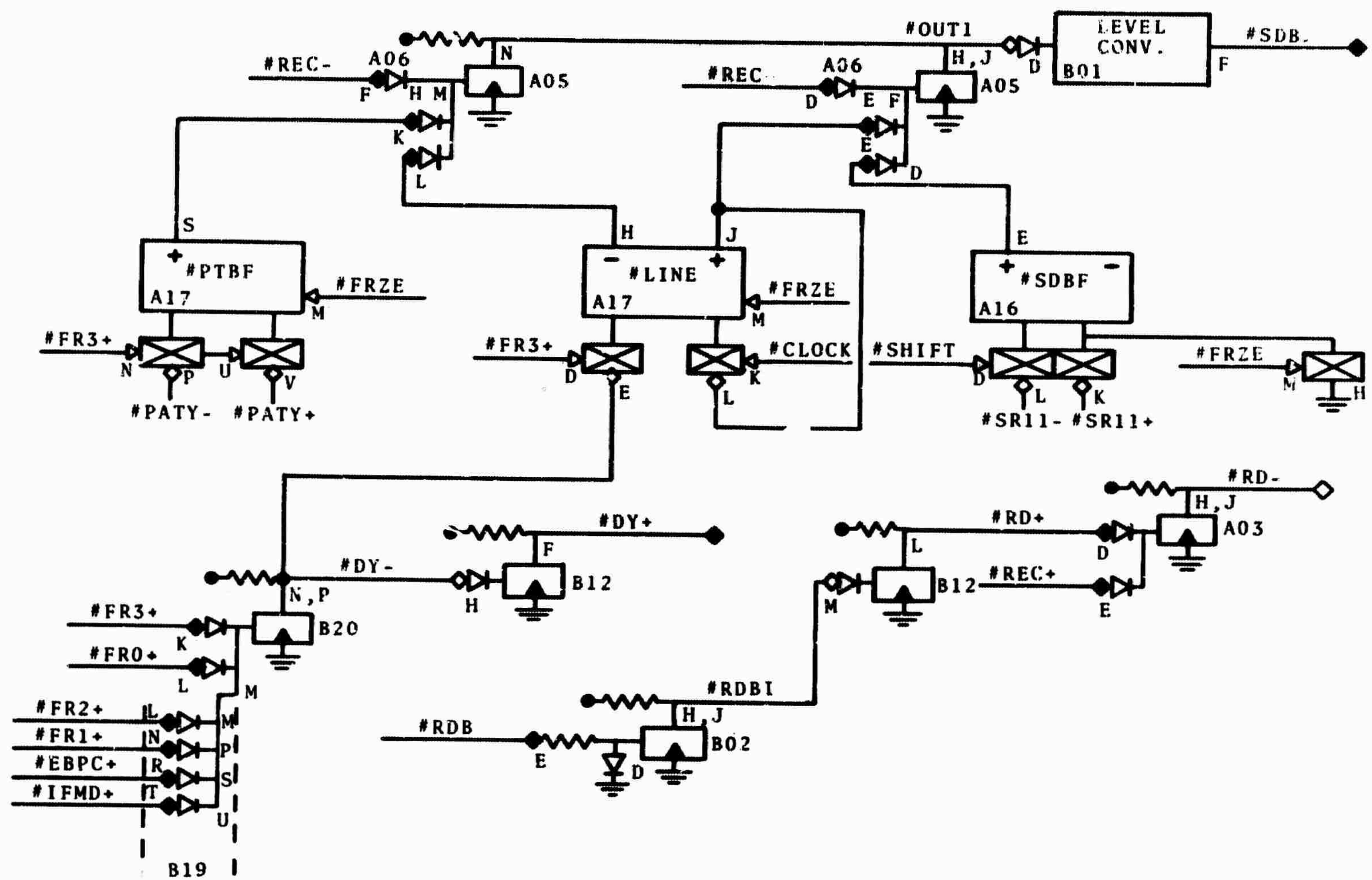

Diagram 5. SDR SERIAL I/O GATING

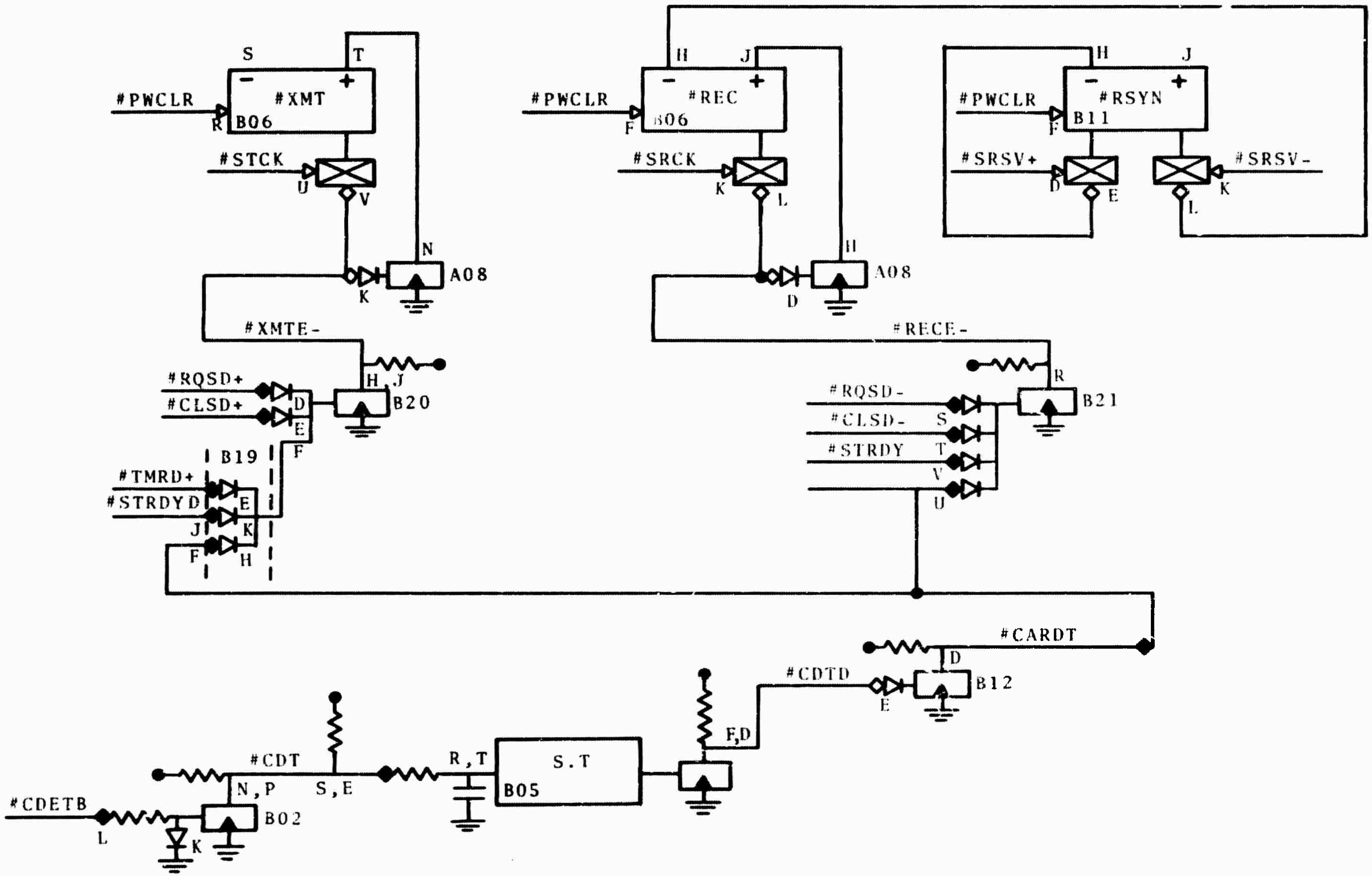

Diagram 6. TRANSMIT/RECEIVE STATE GATING

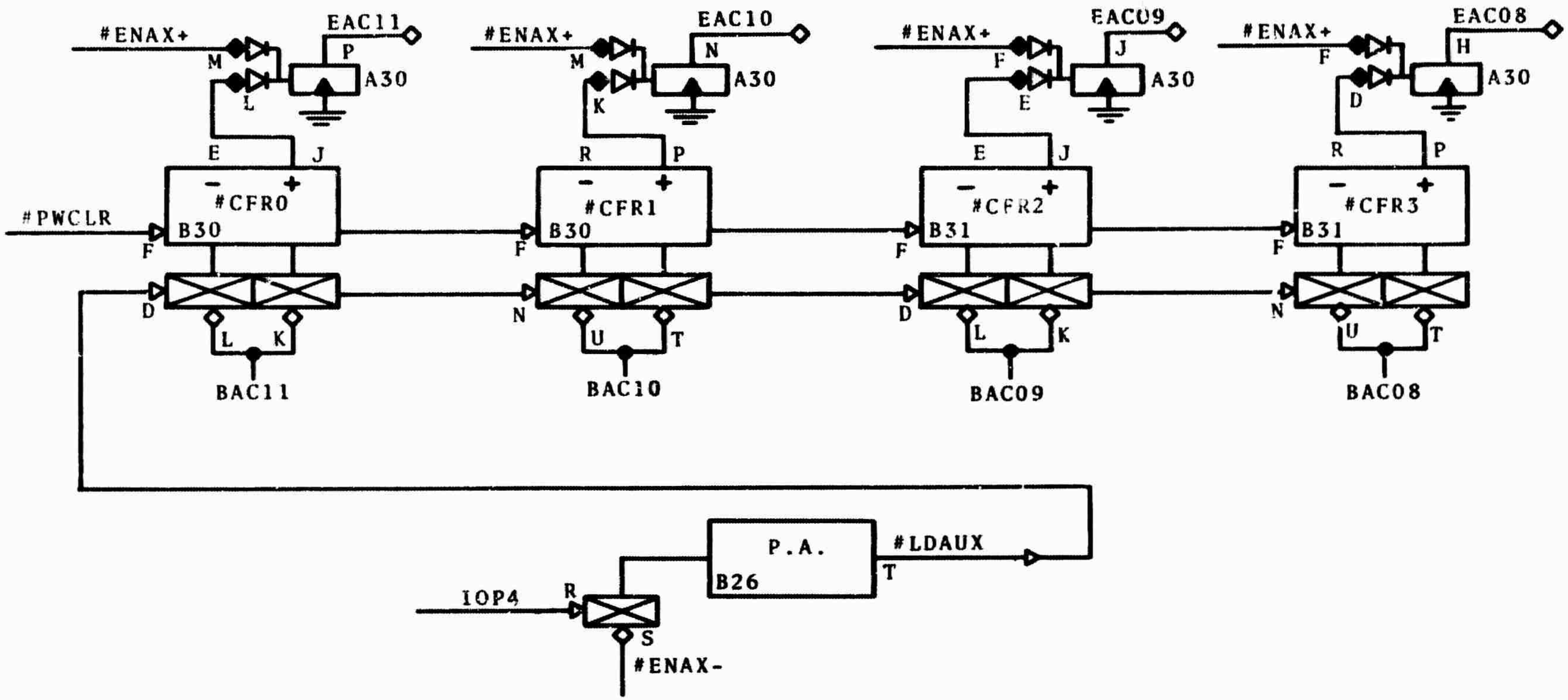

Diagram 7. CONTROL REGISTER 2 (FRAME SIZE)

Frame Counter (Diagram 8)

The frame counter determines by its overflow when a character has been received or transmitted, thus making the positive transition of #FR3+ the character received/transmitted signal. It is reloaded from Control Register 2, each character time making use of the fact that the register is zero at this time. It is thus necessary only to clear the register at the beginning of an operation via the #SVC signal. The frame counter is normally incremented when in the text state and not in a transition state (#SVC+). The #IOPCS signal forces the counter to wait one bit time on character synchronization when parity checking is enabled to take account of the parity bit on the SYN character.

State Synchronization (Diagram 9)

The #SVC state and #SVC-positive transition are used throughout the interface to clear it on a XMT/REC state change or a change in the text state. The remainder of the logic is necessary for its synchronization to the clock signal.

Text State and Sync Detection (Diagram 10)

The text state is embodied in the flip-flop #IFMD. The flip-flop is one bit of Control Word 1 and is therefore accessed through the AC under program control. Two of its other input gates place #IFMD in the correct state when the XMT/REC state is entered. The remaining gate sets #IFMD in the text state when character synchronization is found in the REC state. This transition is conditioned by #DTSY+ and strobed on the clock signal. #DTSY+ is the logic 1-and gate used to determine whether the first 8 bits of the SDR register contain the SYN character.

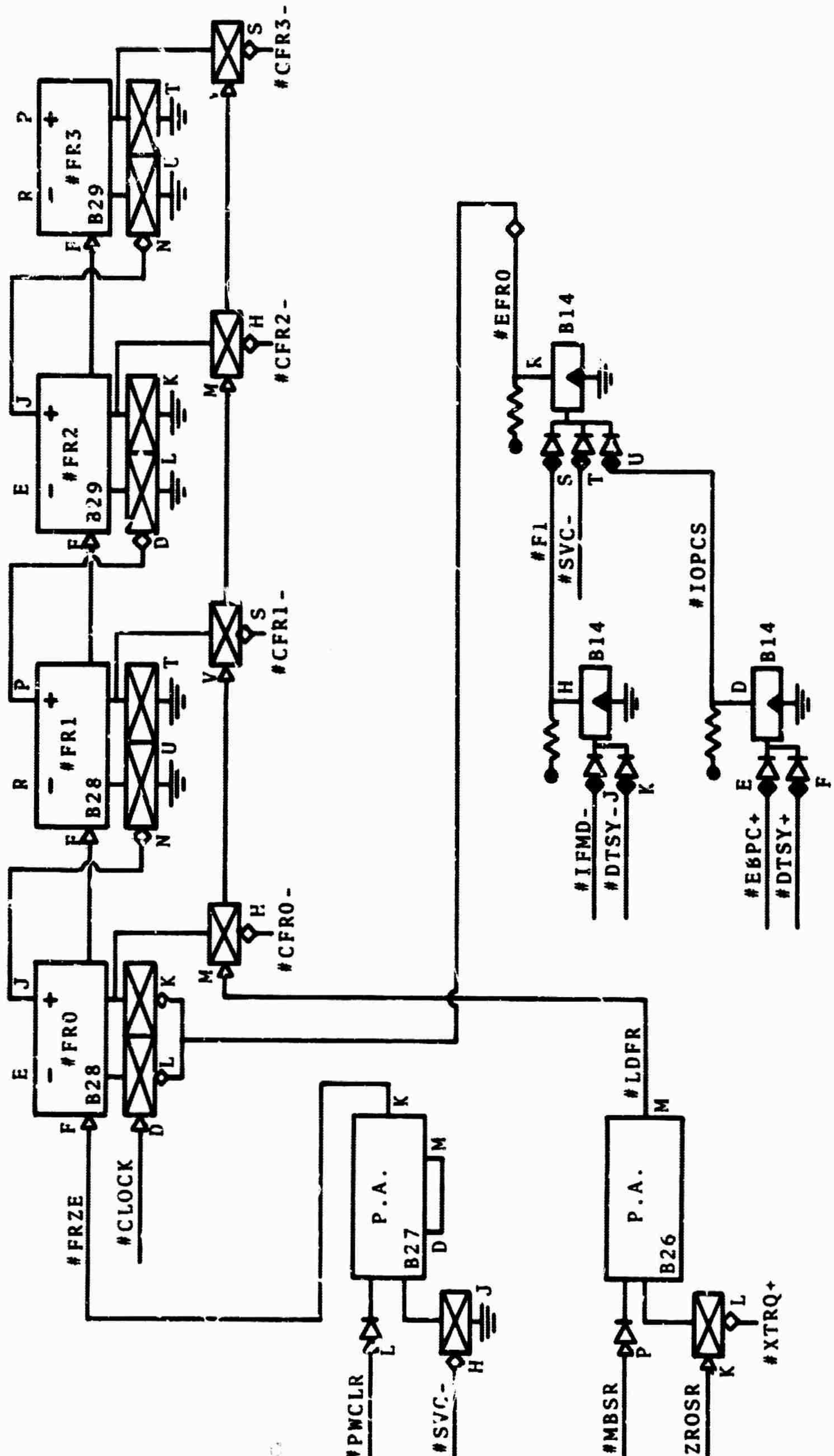

Diagram 8. FRAME COUNTER

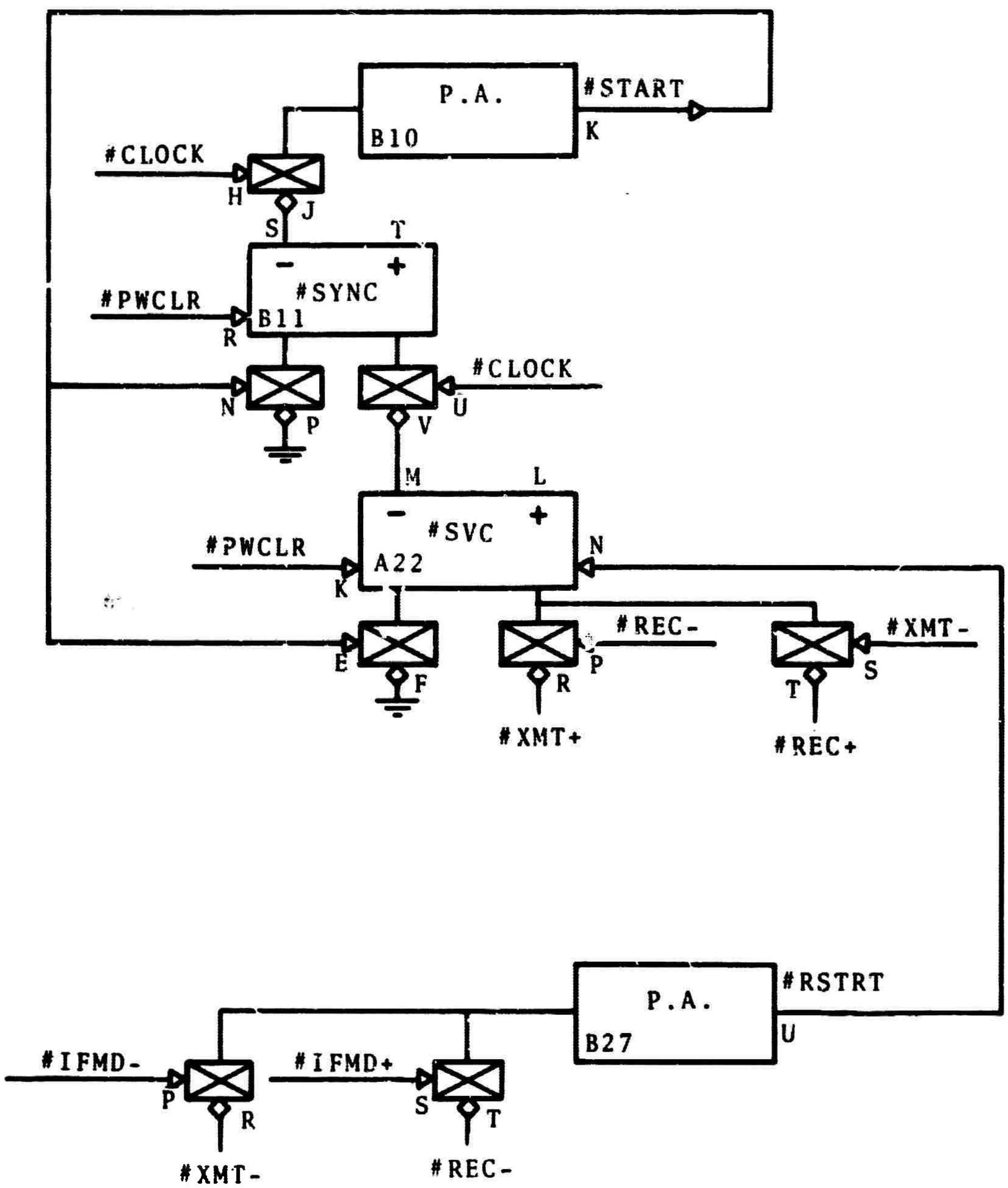

Diagram 9. STATE SYNCHRONIZATION

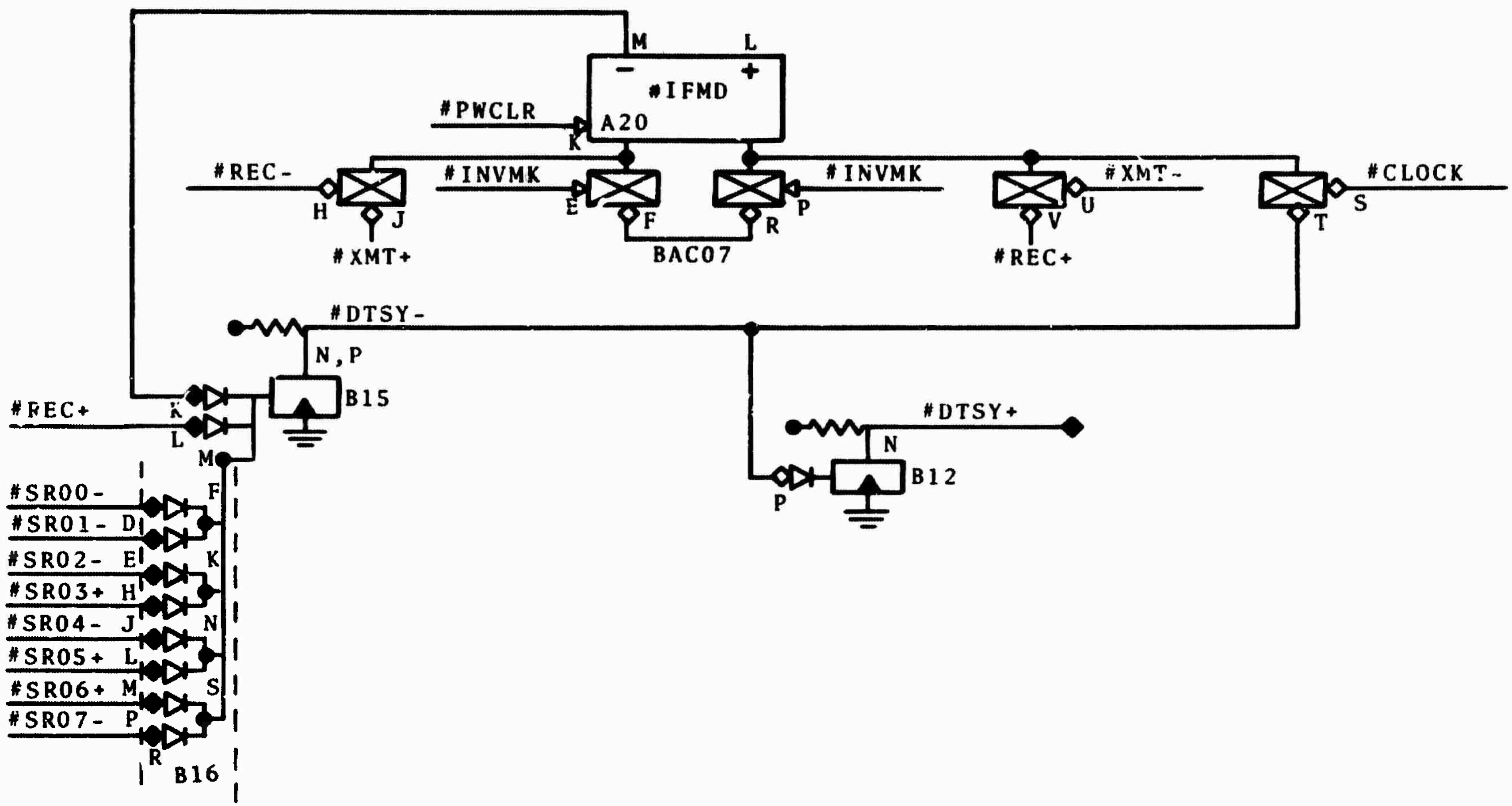

Diagram 10. TEXT STATE AND SYNC DETECTION

Parity Gating (Diagram 11)

The check-vertical-parity-status flip-flop is designated #EBPC in the interface. It is manipulated in the same manner as described above for other bits in Control Word 1. The parity error flip-flop is #PAR and normally is set to zero when #EBPC is not set. When parity checking is enabled, the accumulated parity in #PATY is compared against the last bit of the character when receiving, and #PAR is set if they are not the same.

Clear- and Request-to-Send Gating (Diagram 12)

The contents of the transmit request flip-flop (#XTRQ) is jammed into the request-to-send flip-flop (#RQSD) at the end of each data-break cycle requested by the interface. Since the cleared status of #RQSD is ¬(request-to-transmit) a gate is provided to set #RQSD immediately upon the transition of #XTRQ if the interface is in neither the XMT or REC state. This method of control of request-to-send guarantees that the processing of the current character will be concluded before the XMT/REC state is changed. Furthermore, if #RQSD is set, at least one character must be transmitted before a receive operation can occur.

The clear-to-send indication, #CLSD, is derived from the data set signal #CSDB. In order to avoid a spurious receive state, clear-to-send must be delayed from dropping after request-to-send drops. This delay is necessary because the data set brings up carrier after first dropping it when clear-to-send drops. It appears that this is the result of the data set "flushing" itself after a transmit operation.

Character Service Interrupt Flag (Diagram 13)

The interace's character interrupt flag is #SRSV. This flag is set in the text state on each received character, and in the text state on each character transmitted if there

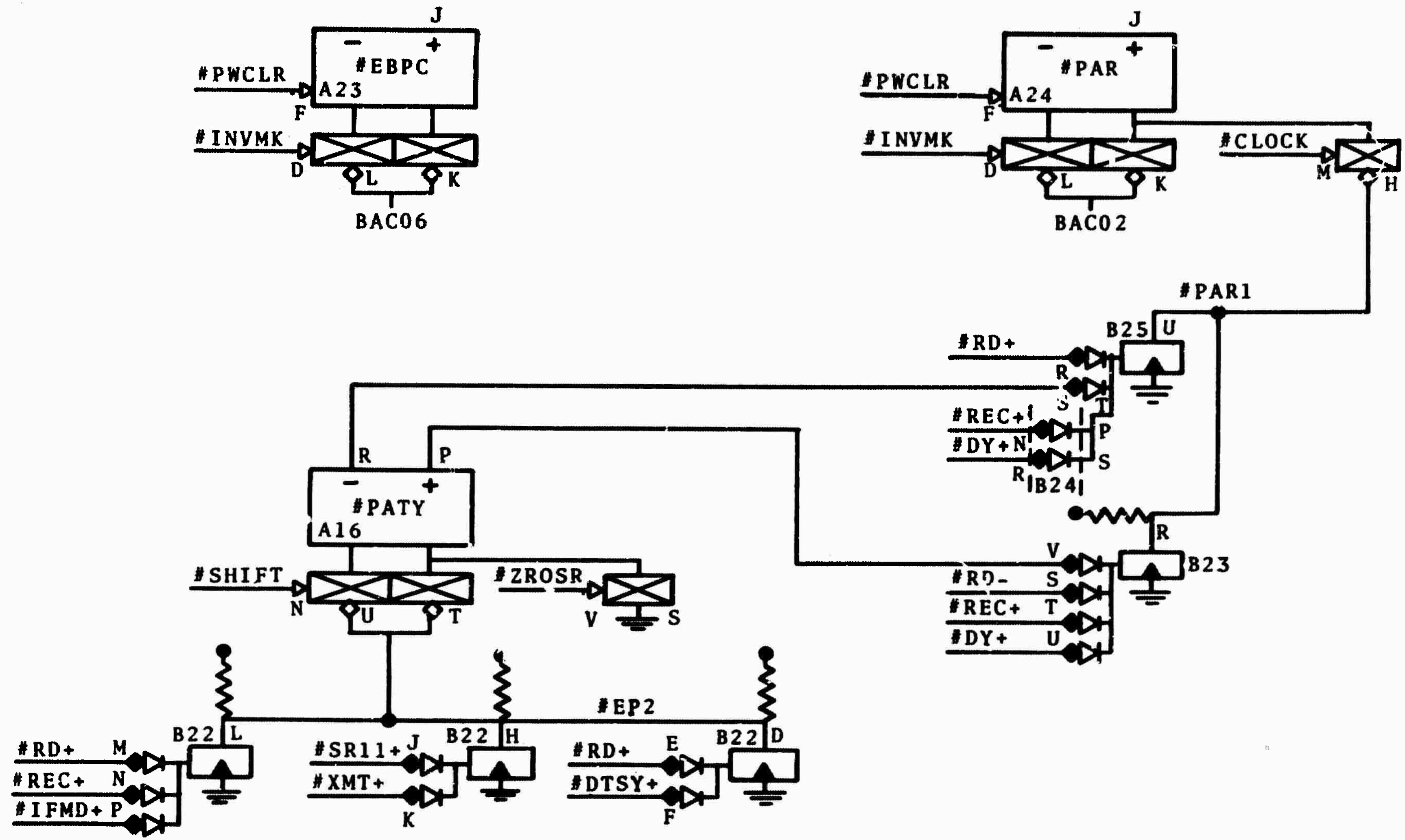

Diagram 11. PARITY GATING

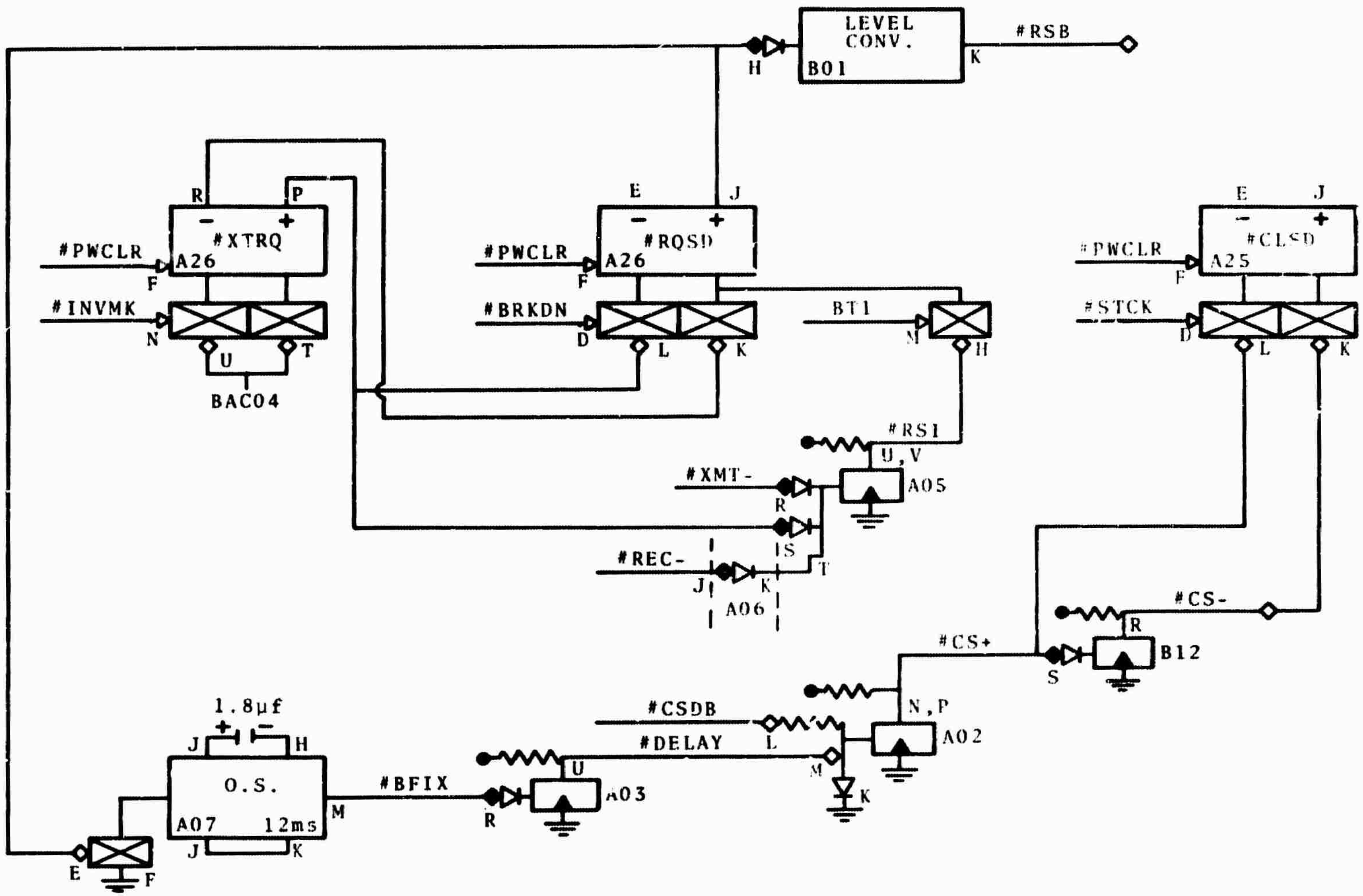

Diagram 12. CLEAR- AND REQUEST-TO-SEND GATING

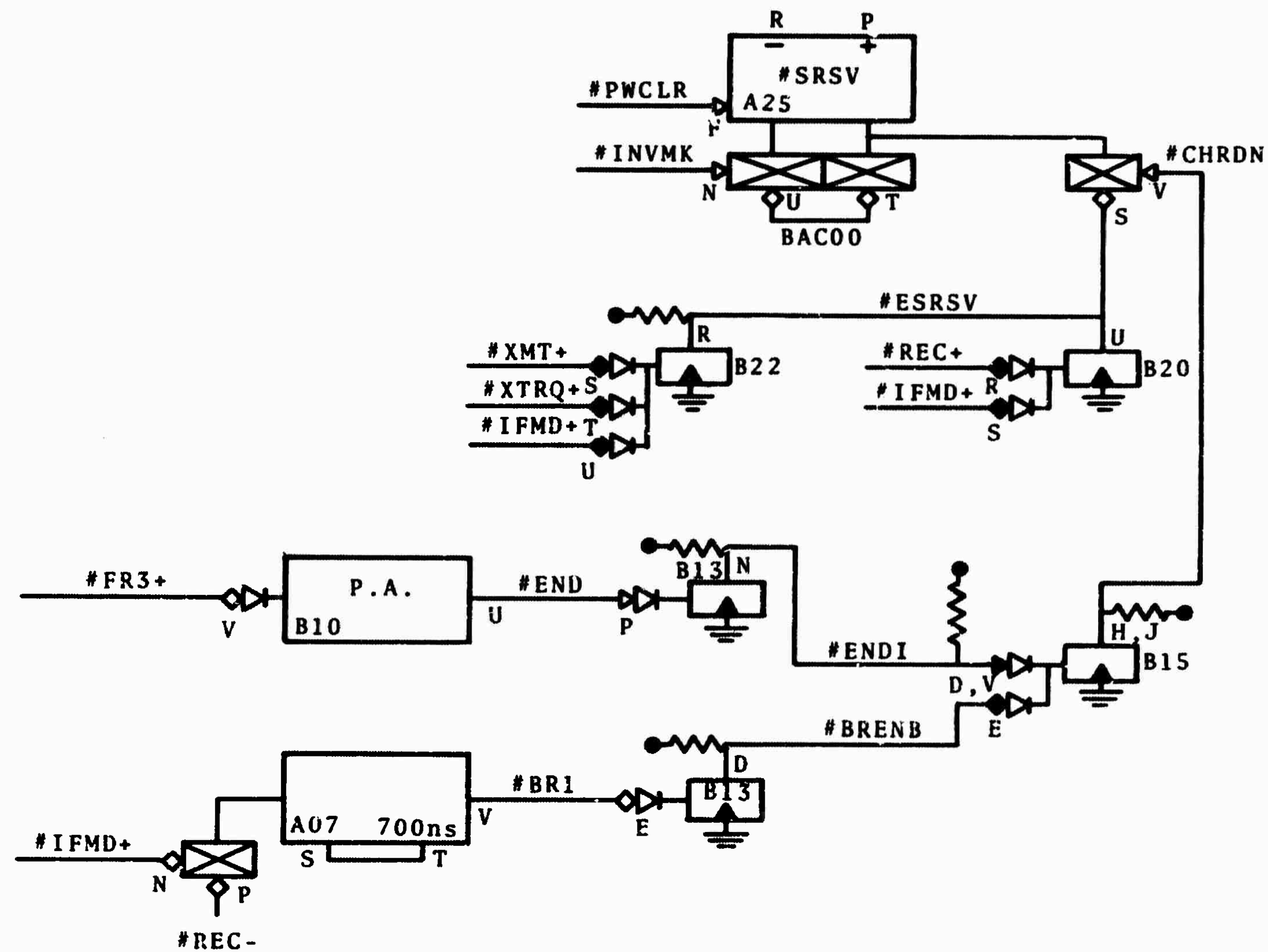

Diagram 13. CHARACTER SERVICE INTERRUPT FLAG

is still a transmit request pending. Every time the frame counter overflows, an #ENDI pulse is generated. This pulse is normally the character service request except when a change in text mode generates a false overflow, thus the need for #BRENB.

<u>Status Indicators</u> (Diagram 14)

Diagram 14 shows the remaining status bits of Control Word 1. Terminal ready (#TMRD) and data lost (#DLST) can be manipulated under program control as described above. Set ready (#STRDY) and (#RING) are only gates since they present static status of the data set.

<u>Control Word 1 EAC Gating</u> (Diagram 15)

Diagram 15 shows the gating necessary to load Control Word 1 on the extended AC buss (EAC).

<u>Miscellaneous Pulses</u> (Diagram 16)

To prevent undue loading of the PDP-8 power clear signal and to allow for reshaping the pulse, #PWCLR is derived. #INVMK is the pulse used to invert under mask the bits in Control Word 1.

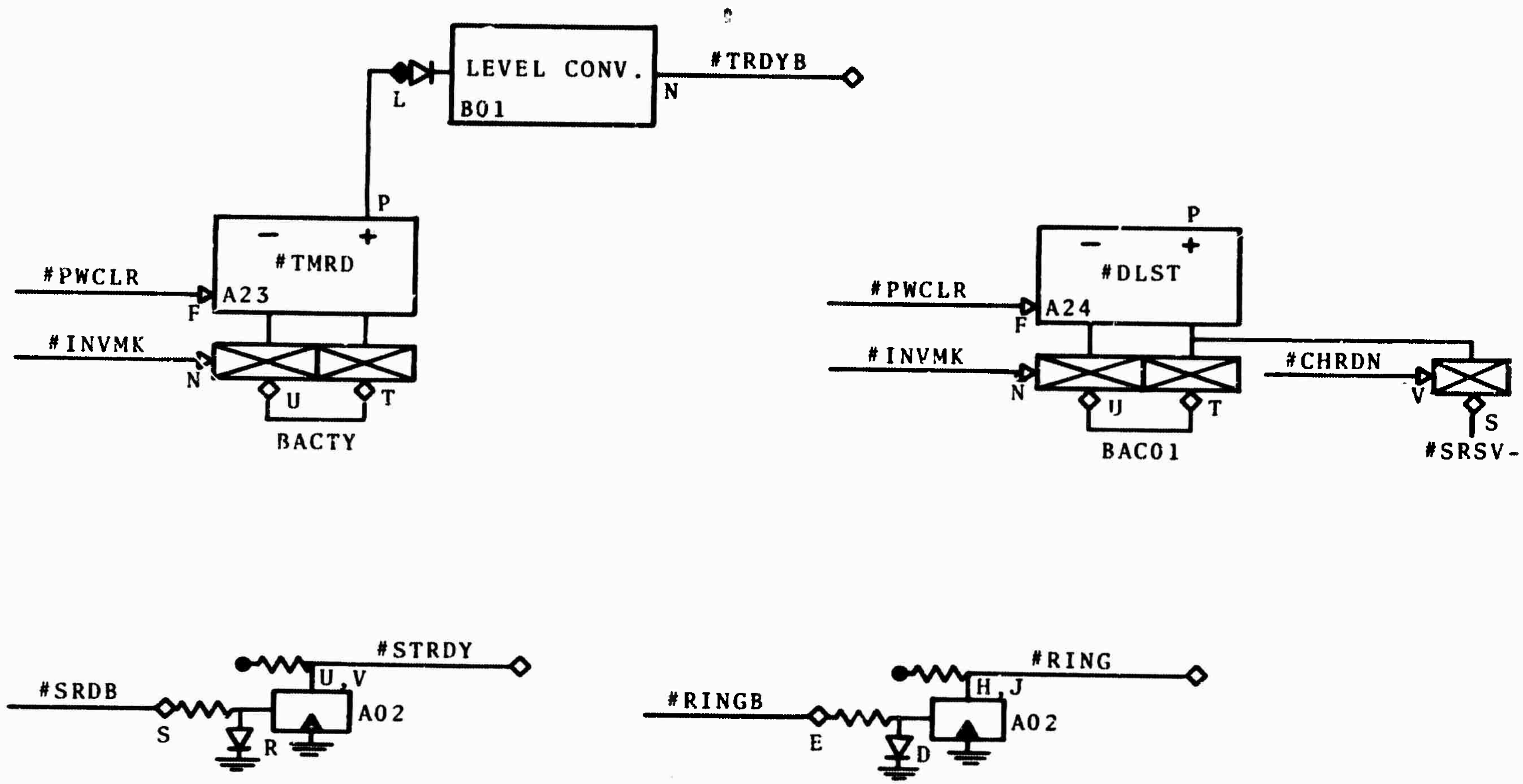

Diagram 14. STATUS INDICATORS

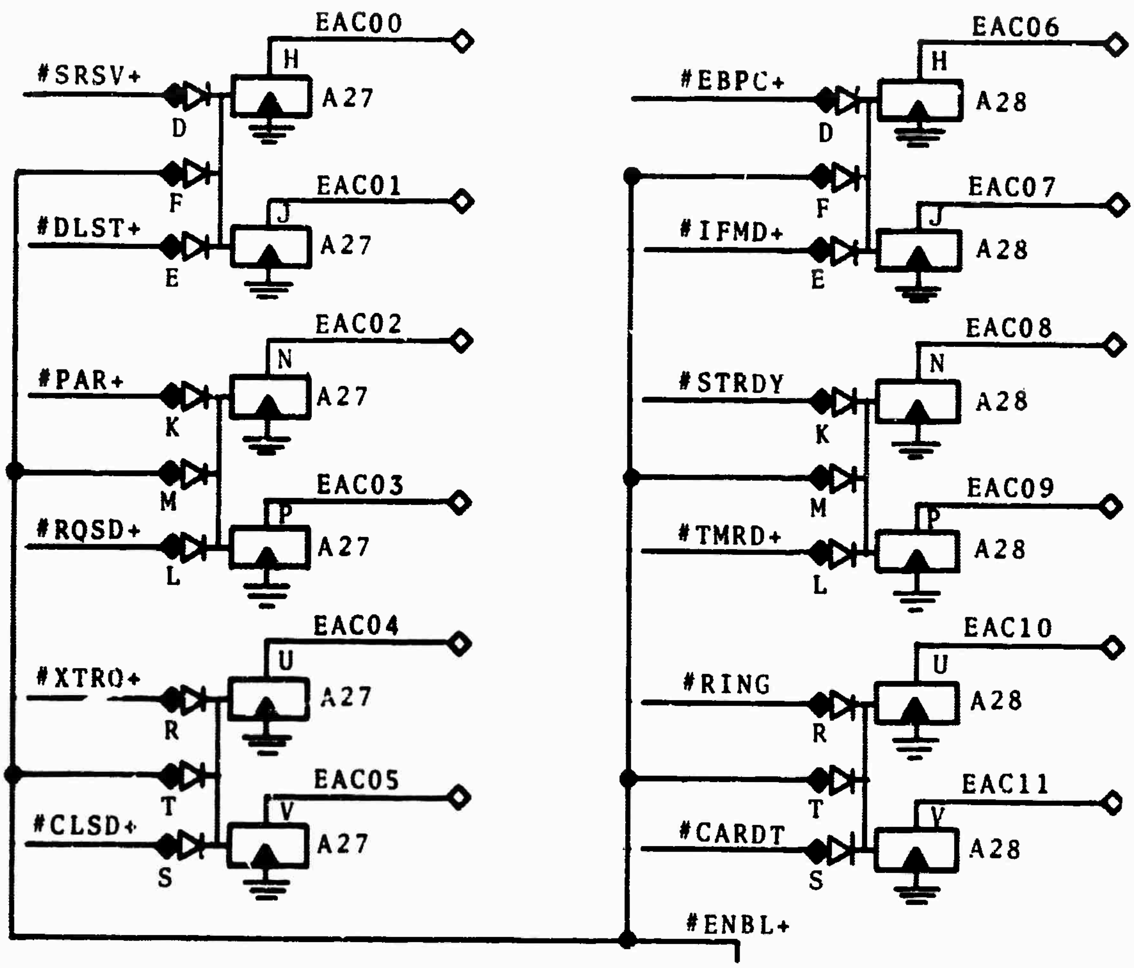

Diagram 15. CONTROL WORD 1 EAC GATING

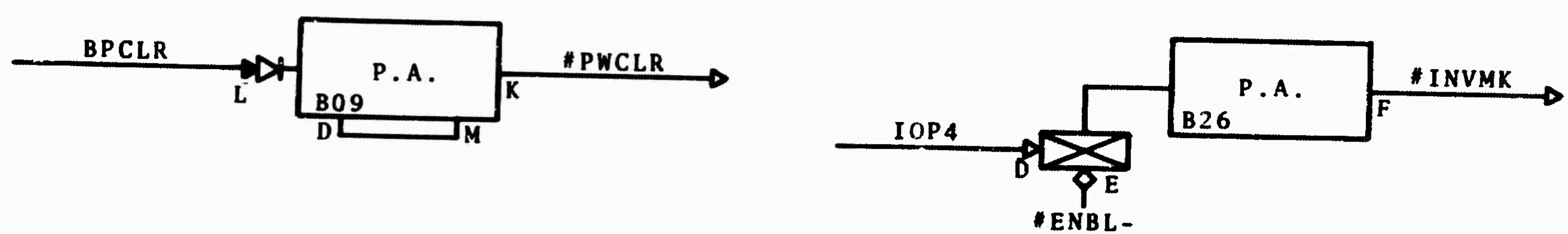

Diagram 16. MISCELLANEOUS PULSES

APPENDIX I

PDP-8/201A LINE ADAPTOR INTERFACE
FOR USE WITH A
PDP-8 WITH THE DATA-BREAK FACILITY

APPENDIX I

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PDP-8/201A LINE ADAPTOR INTERFACE
FOR USE WITH A
PDP-8 WITH THE DATA-BREAK FACILITY

The remainder of the logic and details of the 201A data communication adaptor using the data-break facility is presented in this Appendix. With reference to Figure 1, the body of the logic to be discussed here is considered to make up the PDP-8/201A line adaptor interface.

The total 201A data communications adaptor is realized in two DEC 1943 wire-wrap panels. For the purpose of this report, each panel is called a bay. In this version of the adaptor, for the most part, the PDP-8/201A line adaptor interface is in Bay 1 with the 201A line adaptor in Bay 2. Throughout the remainder of this Appendix, unless noted otherwise, the logic discussed is in Bay 1.

<u>Data Break Control</u> (Diagram I-1)

The line adaptor signals the PDP-8 through the #BKRQ flip-flop that a data transfer is desired to or from PDP-8 core. The address within the PDP-8 memory is read by the PDP-8 from the data address lines. The low-order bit of this address is given by DIAD11. When the break request is given, the direction of the transfer is specified by the DICTL signal. When the PDP-8 enters the break state and the address is loaded into the memory address register, an address accepted pulse is generated by the PDP-8. At this time, the break request signal must be dropped by the interface. During the break state, as defined by the BBREAK signal, the BT1 pulse indicates the end of the break cycle, and is used to strobe the contents of the designated memory location from the buffered memory buffer register into the SDR register. The PDP-8 will also strobe the data-break input lines (DATA BIT) into memory at this time in case the transfer direction is into core. The break request signal is generated each time the frame counter overflows while

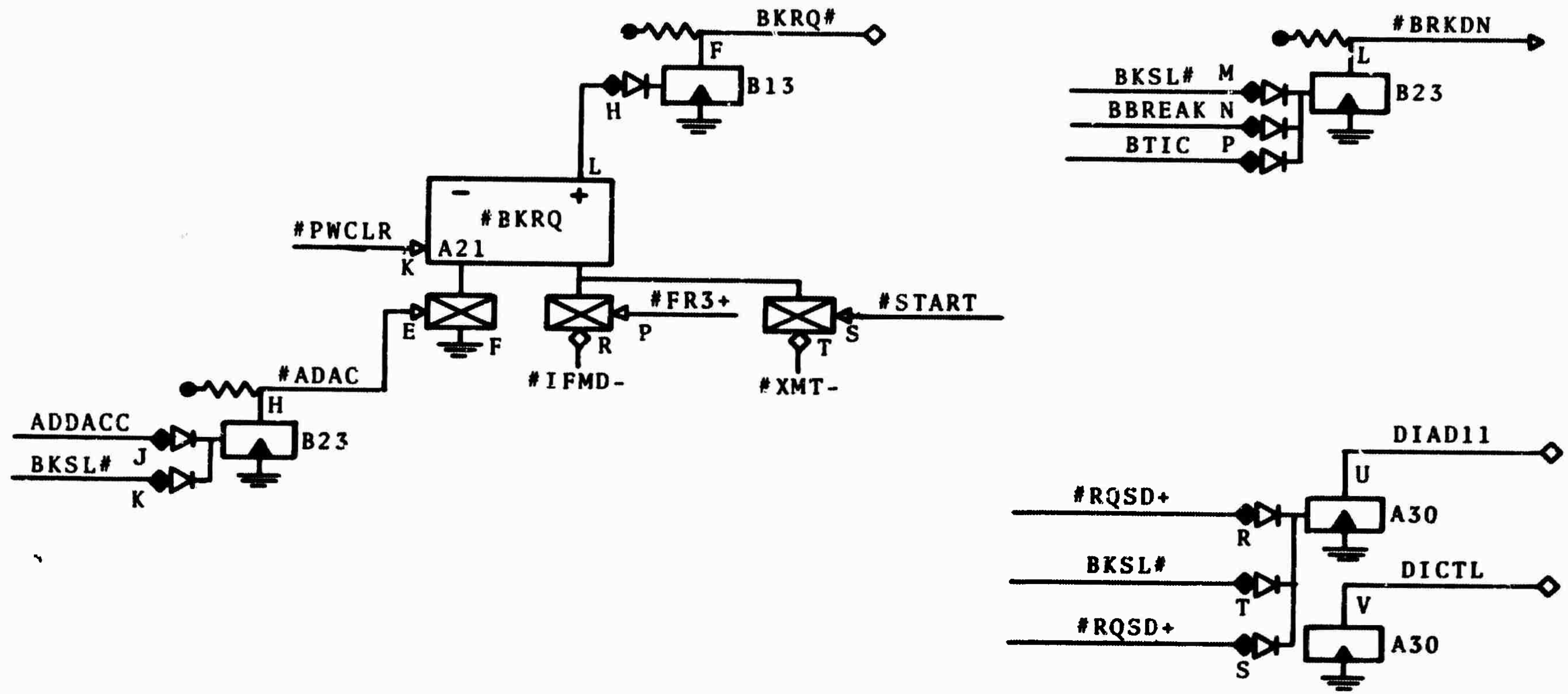

Diagram I-1. DATA-BREAK CONTROL

in the text state, and when the interface first enters the transmit state to fetch the first character to be transmitted. All of the logic shown in this diagram is in Bay 2 of the interface.

<u>Data Break Address</u> (Diagram I-2)

The 201 line adaptor has assigned two sequential locations in PDP-8 core to be used as buffers for incoming (received) and outgoing (transmitted) data. These two locations are specified in the hardware on a W021MG address card. The address is a 14-bit address to allow the buffers to be in any core bank. The 15th or low-order bit is not required because a pair of locations is being specified. By convention, the even location of the pair is the receive buffer and the odd location is the transmit buffer. Using the DEC numbering convention, the address is given by the vector ADDR(0)...ADDR(14). Schematically, the W021MG module is shown in Figure I-1.

These address lines are then buffered as shown in Diagram I-2 and form the inputs for the data break address (DADR); the low-order bit (DIAD11) is generated by the request-to-send signal and is shown in Diagram I-1.

The j-th position (j=0,...,13) of the address is a 0 if there is a jumper to ground at that position and is a 1 otherwise. The W021MG address card is located in module position 1B09. If any of the three high-order positions (ADDR(0), ADDR(1), or ADDR(2)) is a 1, there must be extended memory capabilities on the PDP-8, and the eleventh or address extension cable must be provided.

<u>Device Select Code</u> (Diagram I-3)

The device select code is a two octal digit number which selects an external device during an input/output operation. The device code appears in positions 3 through 8 of the memory buffer (M.B.) during an IOT instruction, alerting the external device that it is being selected.

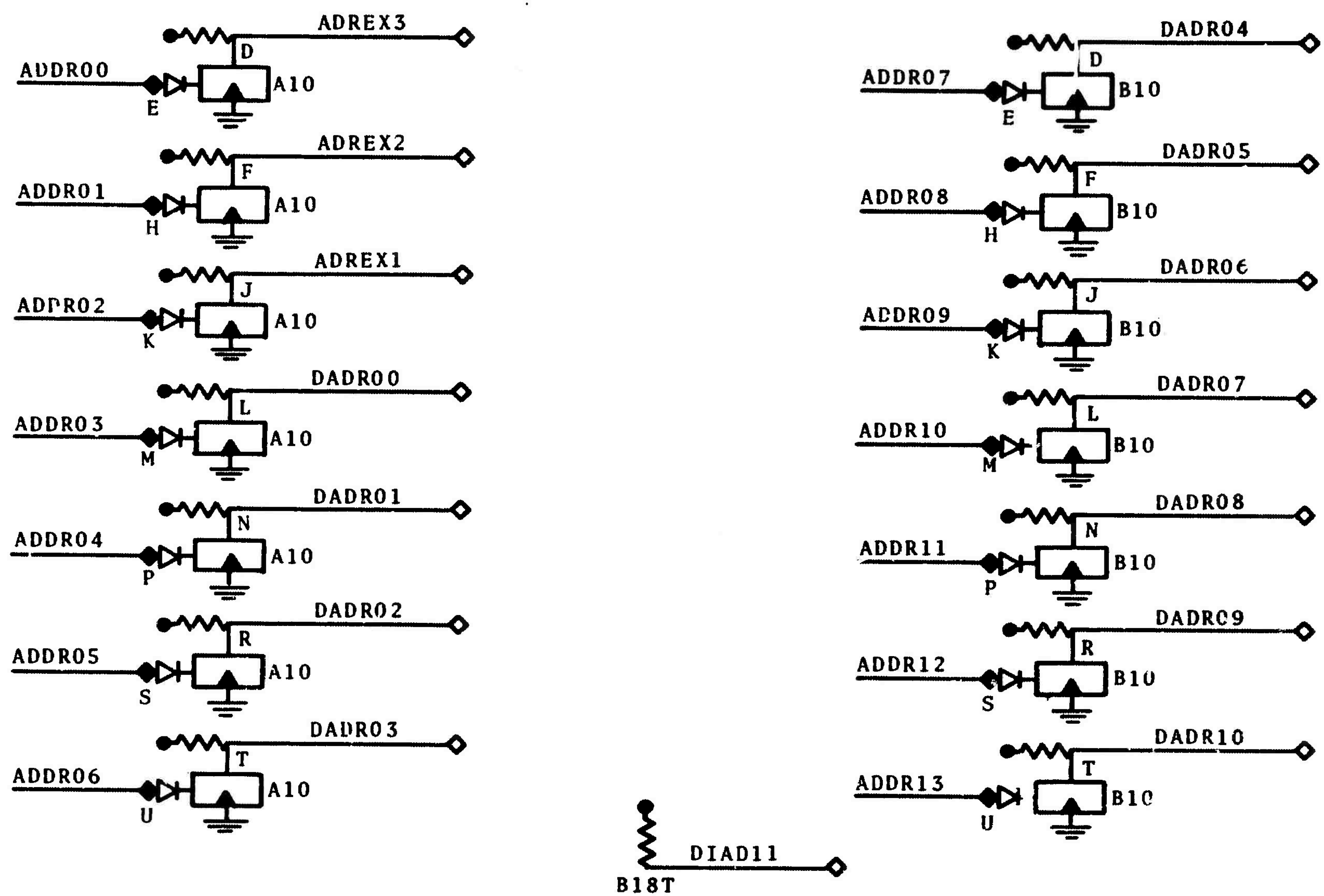

Diagram I-2. DATA-BREAK ADDRESS LINES

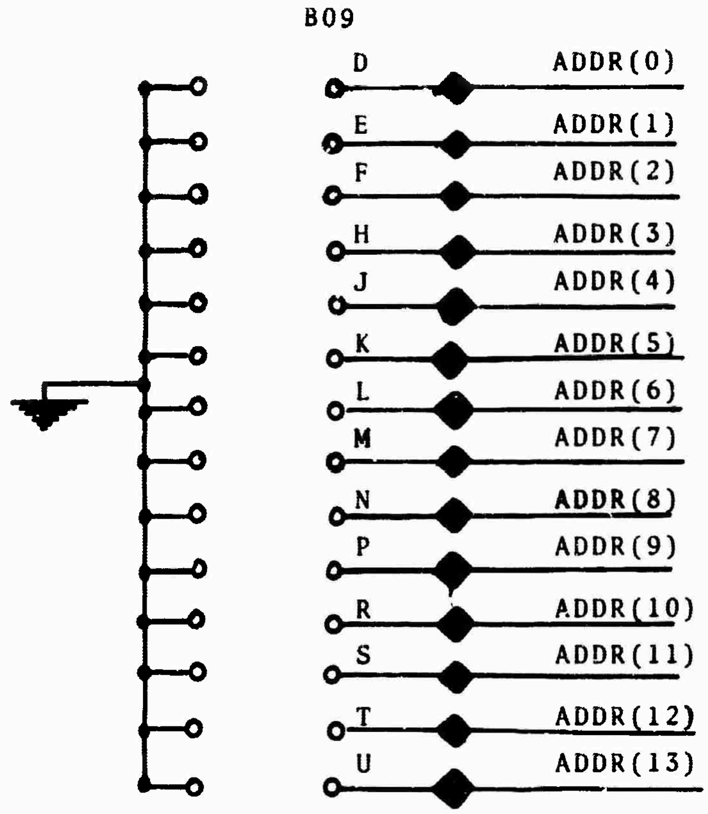

Figure I-1. W021MG Address Card.

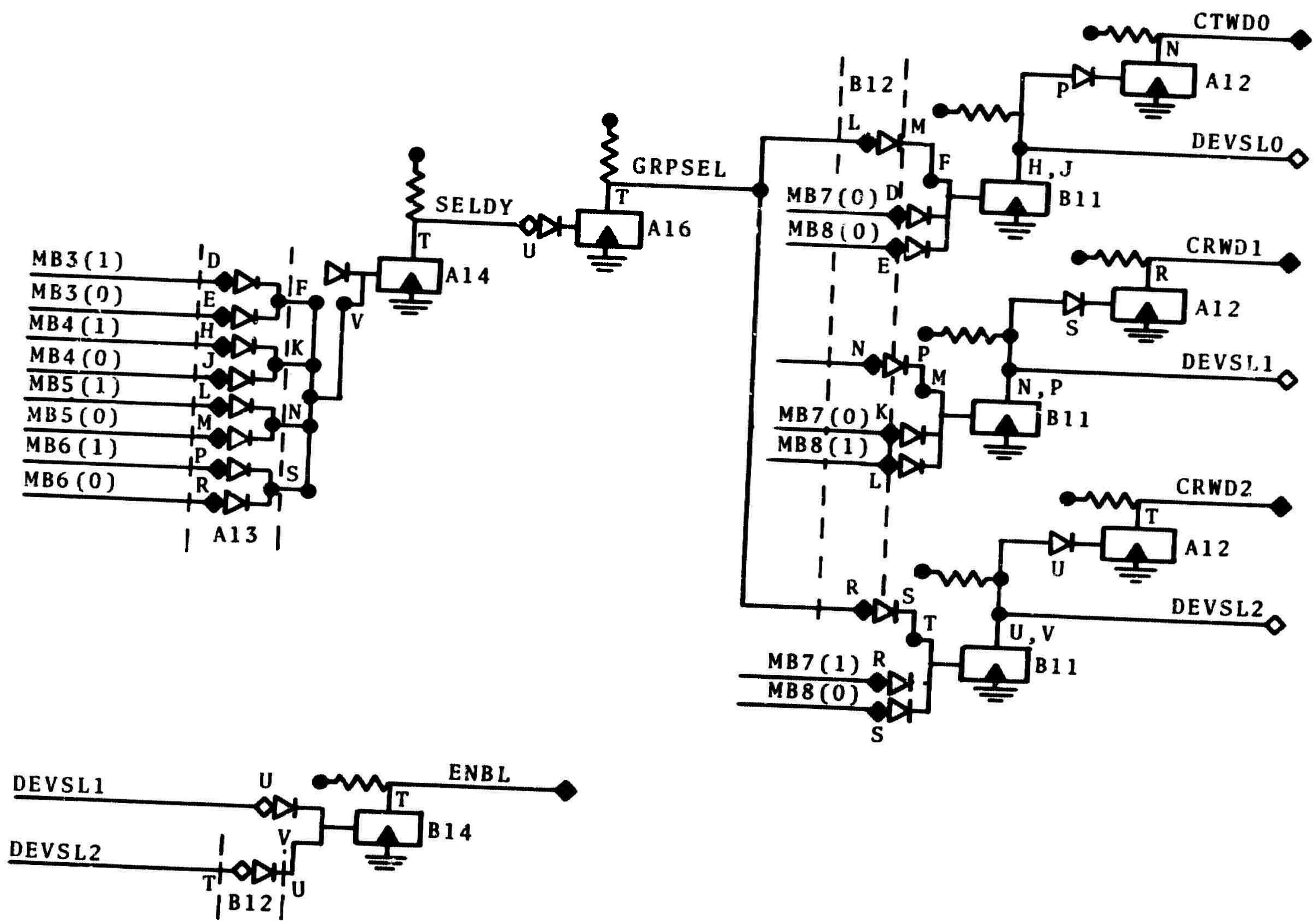

Diagram I-3. DEVICE DECODING

The 201A L.A. has associated with it three separate device codes as discussed above. In order to specify the three devices it is sufficient, because of the aforementioned requirements, to define only a four-bit number, which appears in positions 3-6 of the M.B. during an IOT instruction. This number must also be realized in the hardware, and this is accomplished via an R002 diode module found in position 1A13 and pictured at the far left of Diagram I-3.

Thus to specify the desired set of device codes the appropriate diodes are removed. For example, using the set 40, 41, 42 as before, the diodes connected to pins E, H, L, and P must be removed.

The remainder of Diagram I-3 shows the gating necessary to obtain the signals to identify each of the devices.

Device Selection Gating (Diagram I-4)

The gates shown in Diagram I-4 are located in Bay 2 and provide the signals to differentiate between Control Word 1 and Control Word 2 operation.

Interrupt Control (Diagram I-5)

Every time a character is transferred between the 201A L.A. and the PDP-8's memory, a character service flag (#SRSV) is set as described above.

This flag in turn sets the appropriate interrupt flag, Transmit (XINT) or Receive (RINT), which causes an interrupt request. If interrupts are enabled in the PDP-8, a program interrupt is generated. Via the appropriate IOT micro-instruction, the program can identify the device causing the interrupt. The SKIP signal will be generated, and a program skip forced if this IOT is executed. It is the program's responsibility to clear the interrupt after it is identified, and the remainder of the gates allow for this.

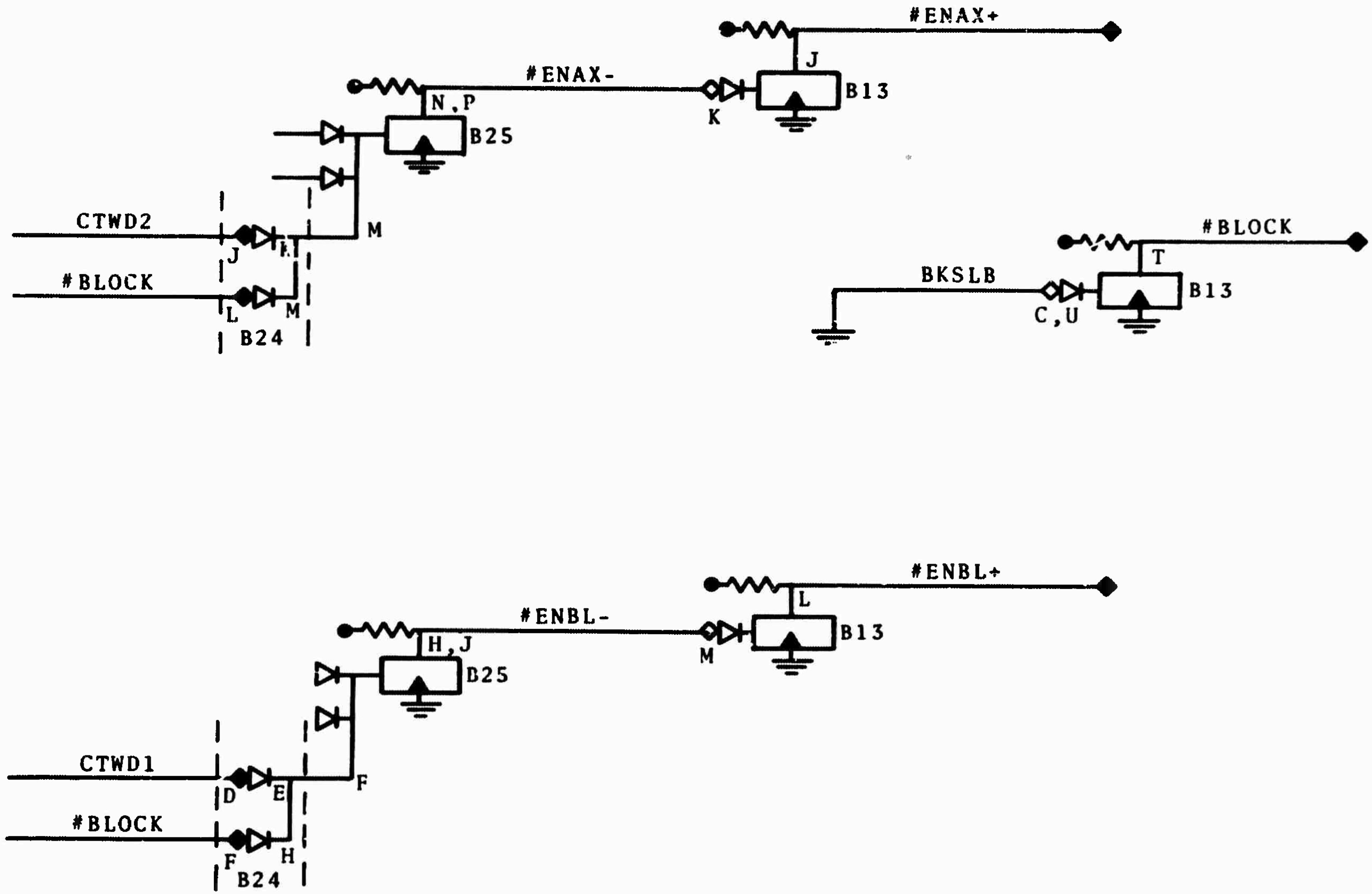

Diagram I-4. DEVICE SELECTION GATING

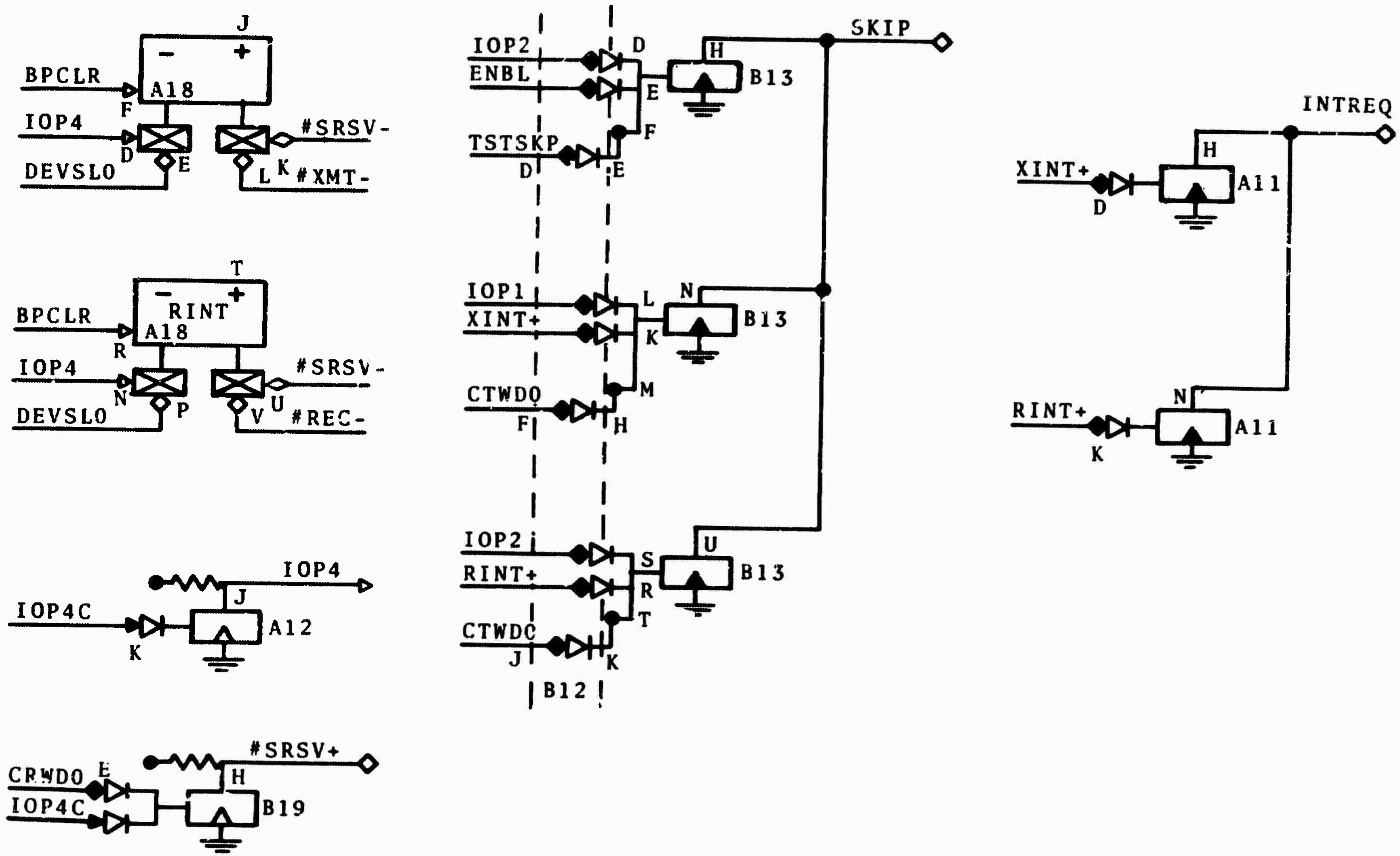

Diagram I-5. INTERRUPT CONTROL

Extended Accumulator Control (Diagram I-6)

In order to provide the IOT structure described in the Programming and Control Considerations section, the Extended Accumulator (EAC) buss was implemented. The full power of the EAC is not realized until multiple devices are using the buss, since it provides the mechanism for multiple inputs to the PDP-8 AC. Diagram I-6 shows the gating necessary to generate the SKIP signal when a skip under mask IOT is executed

Accumulator Input Gating (Diagram I-7)

Diagram I-7 shows the buffers which gate the EAC buss onto the AC buss. For other devices to use the EAC buss they need only provide the appropriate input to the ENBL gate and the gates for the EAC buss.

Extended Accumulator Buffers (Diagram I-8)

Diagram I-8 shows a set of buffers necessary to accomplish the inversion to gate the EAC onto the AC. The clamped loads for the EAC buss are also indicated.

Data Bit Buffers (Diagram I-9)

Diagram I-9 shows the buffers used to provide isolation between the SDR register outputs and the data inputs on a data break into the PDP-8. There is no gating signal provided on these buffers since this is the only device using the data bit lines.

Miscellaneous Circuits (Diagram I-10)

Diagram I-10 is best described as the left-over circuits without a logical home.

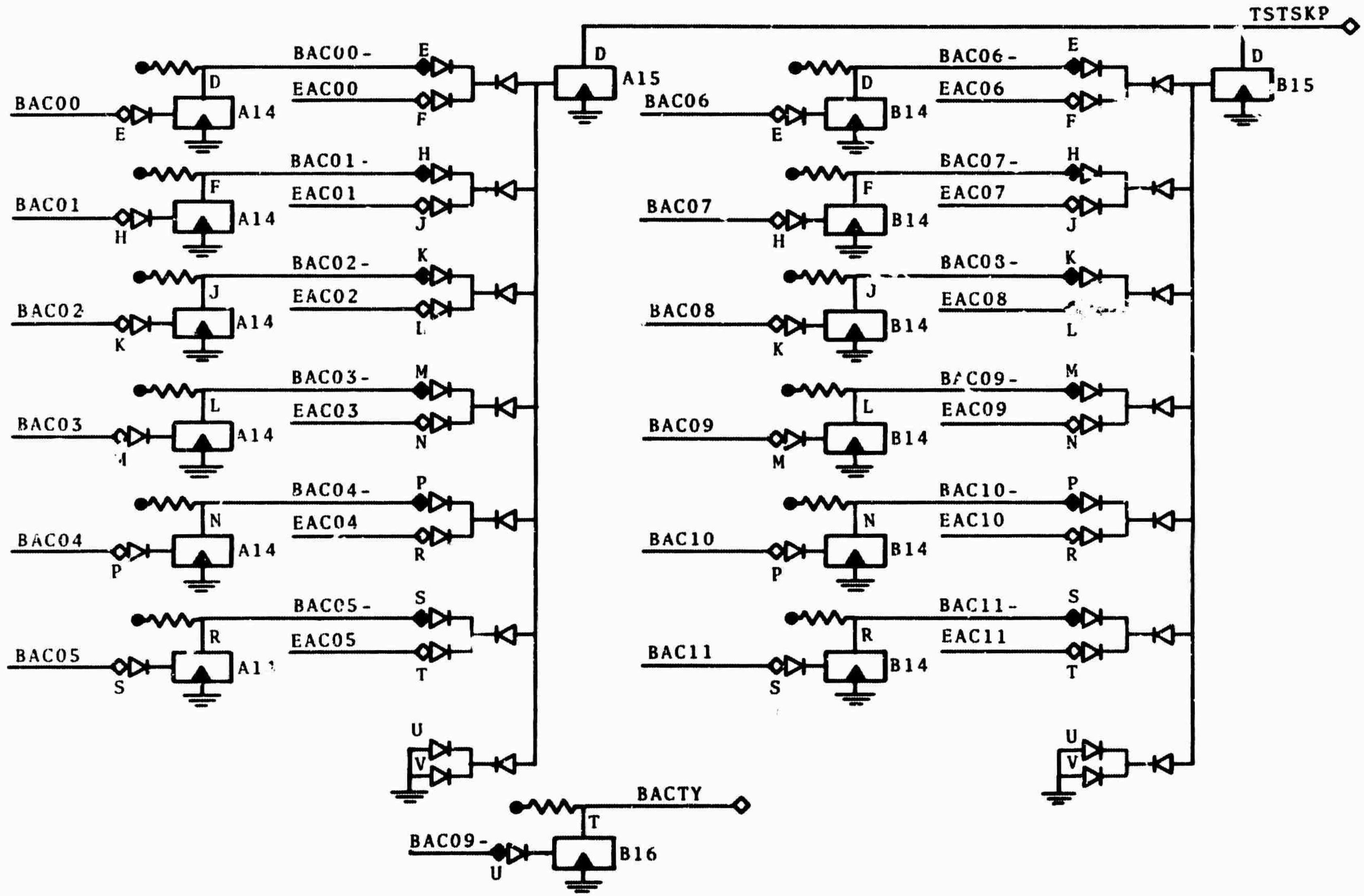

Diagram I-6. EXTENDED ACCUMULATOR CONTROL

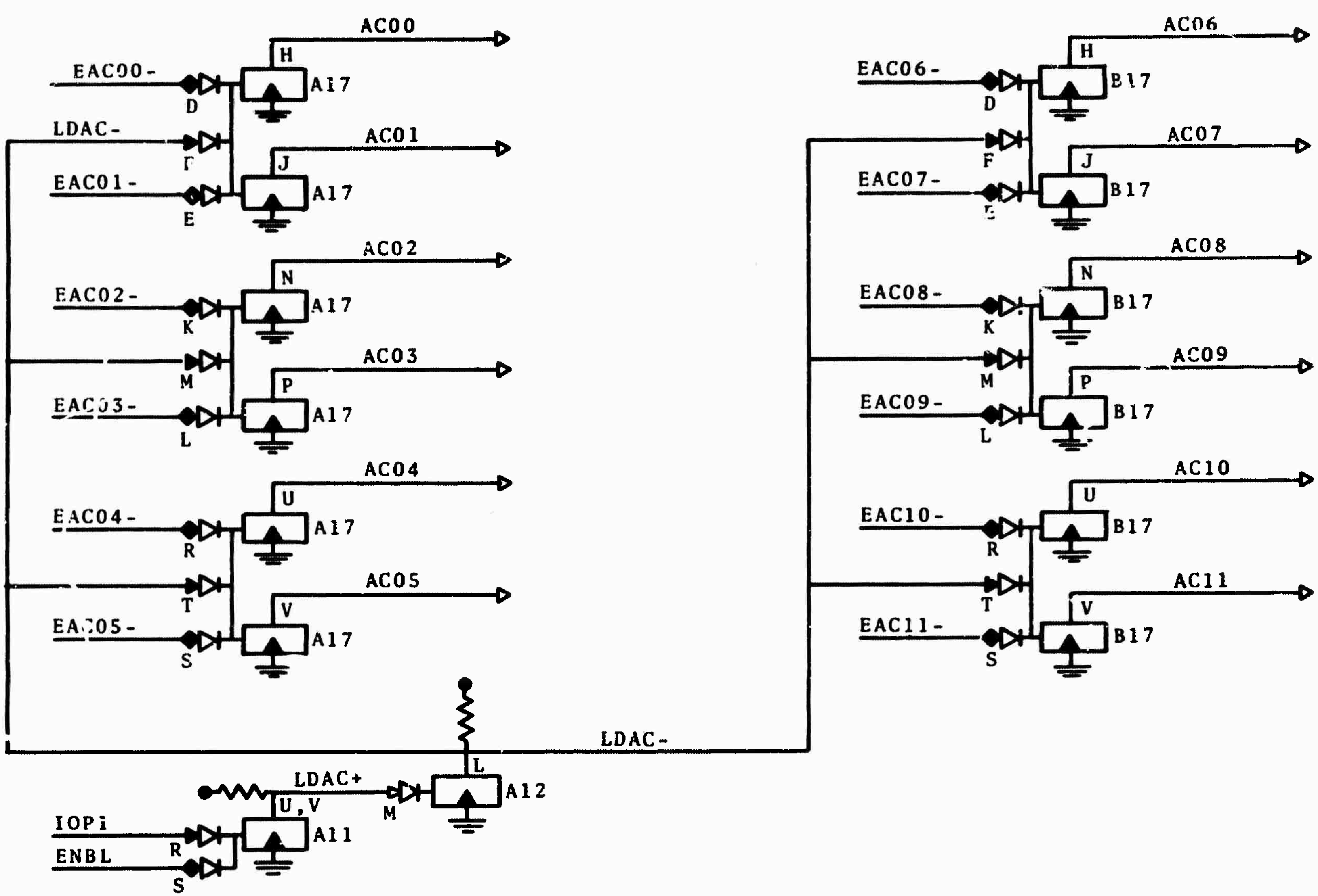

Diagram I-7. ACCUMULATOR INPUT GATING

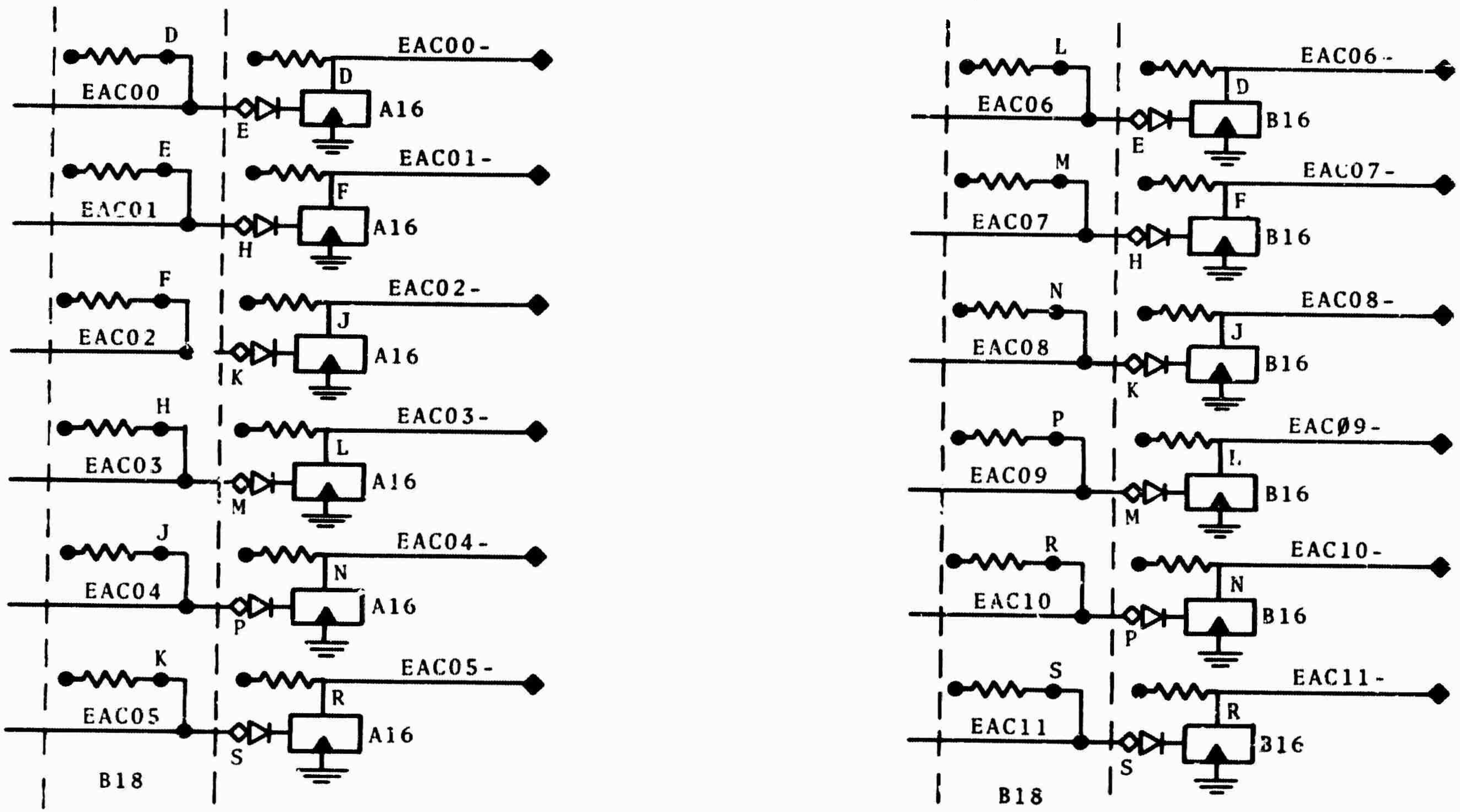

Diagram I-8. EXTENDED ACCUMULATOR BUFFERS

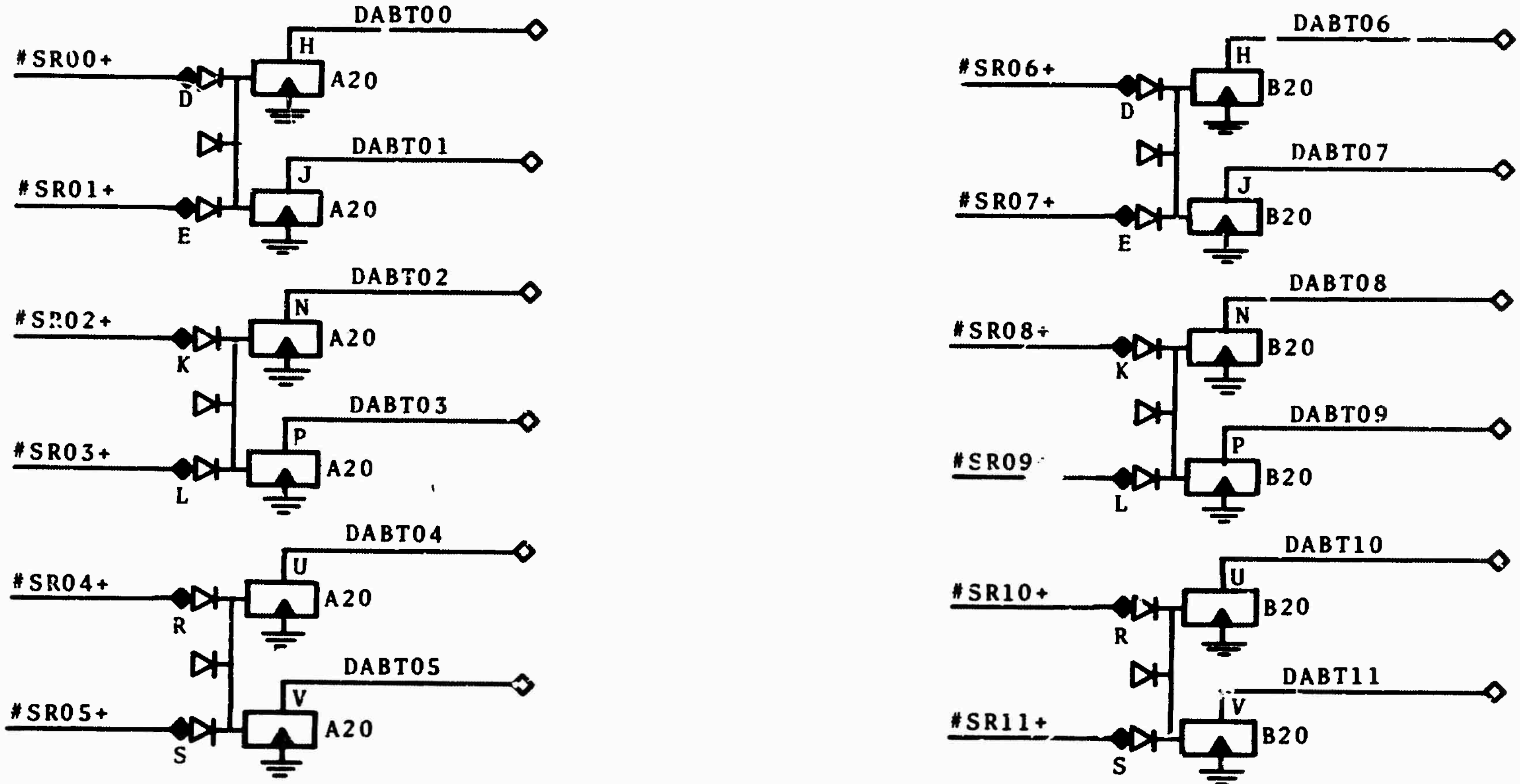

Diagram I-9. DATA BIT BUFFERS

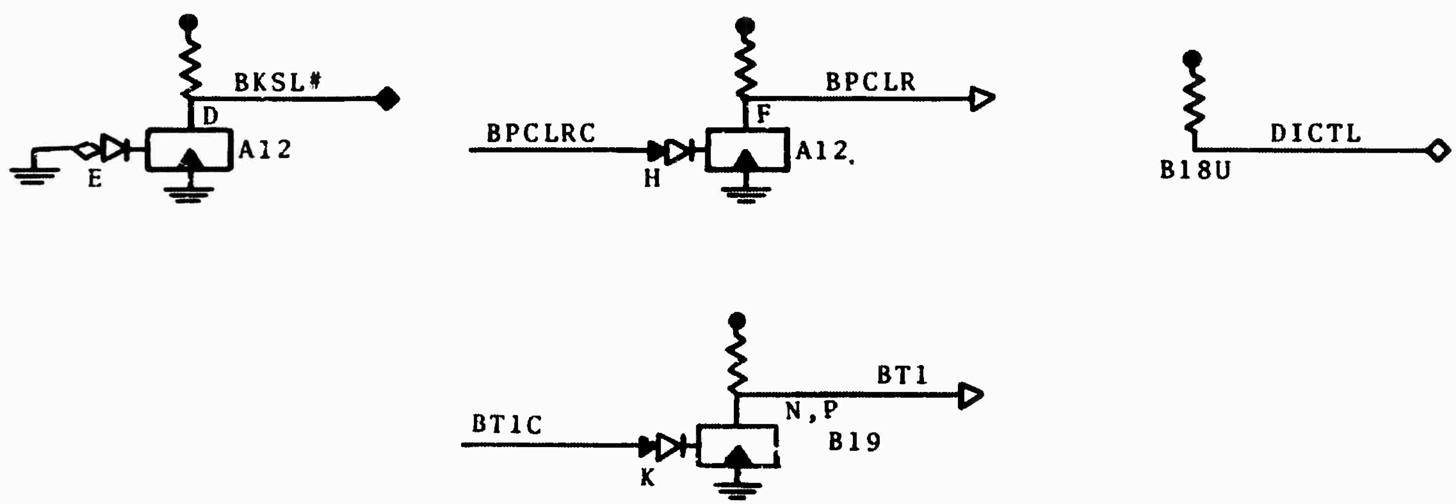

Diagram I-10. MISCELLANEOUS CIRCUITS

Cable Layout (Diagram I-11)

The input/output cables for the 201A L.A. are shown in Diagram I-11. The correspondences between the signal names, module positions, and pin connections for the 201A L.A. and the PDP-8 are given in Tables I-1 through I-7.

Module Utilization (Tables I-8 through I-11)

Tables I-8 through I-11 give the module utilization for a 201A L.A. In addition to the module utilization, a complete signal name map is also shown.

'A'

	01 02	03 04	05 06	07	08	09
D	BAC00	BMB00	AC00	DADR00	DABT00	ADREX1
E	BAC01	BMB01	AC01	DADR01	DABT01	ADREX2
F						
H	BAC02	BMB02	AC02	DADR02	DABT02	ADREX3
J						
K	BAC03	BMB03-	AC03	DADR03	DABT03	
L						
M	BAC04	BMB03	AC04	DADR04	DABT04	
N						
P	BAC05	BMB04-	AC05	DADR05	DABT05	
R						
S	BAC06	BMB04	AC06	DADR06	DABT06	
T	BAC07	BMB05-	AC07	DADR07	DABT07	
U						
V	BAC08	BMB05	AC08	DADR08	DABT08	

'B'

	01 02	03 04	05 06	07	08
D	BAC09	BMB06-	AC09	DADR09	DABT09
E	BAC10	BMB06	AC10	DADR10	DABT10
F					
H	BAC11	BMB07-	AC11	DIAD11	DABT11
J					
K	IOP1	BMB07	SKIP	BKRQ#	
L					
M	IOP2	BMB08-	INT REQ	DICTL	
N					
P	IOP4C	BMB08		BBREAK	
R					
S	BT1C	BMB09		ADDACC	
T	BT2A	BMB10			
U					
V	BPCLRC	BMB11			

Diagram I-11. CABLE LAYOUT

TABLE I-1

BUFFERED ACCUMULATOR OUTPUTS

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A01D, A02D	BAC00			BAC0	ME34D
A01E, A02E	BAC01			BAC1	ME34E
A01H, A02H	BAC02			BAC2	ME34H
A01K, A02K	BAC03			BAC3	ME34K
A01M, A02M	BAC04			BAC4	ME34M
A01P, A02P	BAC05			BAC5	ME34P
A01S, A02S	BAC06			BAC6	ME34S
A01T, A02T	BAC07			BAC7	ME34T
A01V, A02V	BAC08			BAC8	ME34V
B01D, B02D	BAC09			BAC9	MF34D
B01E, B02E	BAC10			BAC10	MF34E
B01H, B02H	BAC11			BAC11	MF34H

TABLE I-2

BUFFERED MEMORY BUFFER OUTPUT LINES

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A03D, A04D	BMB00	—◇	—◇	BMB0(1)	ME35D
A03E, A04E	BMB01	—◇	—◇	BMB1(1)	ME35E
A03H, A04H	BMB02	—◇	—◇	BMB2(1)	ME35H
A03K, A04K	BMB03-	—◇	—◇	BMB3(0)	ME35K
A03M, A04M	BMB03	—◇	—◇	BMB3(1)	ME35M
A03P, A04P	BMB04-	—◇	—◇	BMB4(0)	ME35P
A03S, A04S	BMB04	—◇	—◇	BMB4(1)	ME35S
A03T, A04T	BMB05-	—◇	—◇	BMB5(0)	ME35T
A03V, A04V	BMB05	—◇	—◇	BMB5(1)	ME35V
B03D, B04D	BMB06-	—◇	—◇	BMB6(0)	MF35D
B03E, B04E	BMB06	—◇	—◇	BMB6(1)	MF35E
B03H, B04H	BMB07-	—◇	—◇	BMB7(0)	MF35H
B03K, B04K	BMB07	—◇	—◇	BMB7(1)	MF35K
B03M, B04M	BMB08-	—◇	—◇	BMB8(0)	MF35M
B03P, B04P	BMB08	—◇	—◇	BMB8(1)	MF35P
B03S, B04S	BMB09	—◇	—◇	BMB9(1)	MF35S
B03T, B04T	BMB10	—◇	—◇	BMB10(1)	MF35T
B03V, B04V	BMB11	—◇	—◇	BMB11(1)	MF35V

TABLE I-3

ACCUMULATOR INPUTS

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A05D, A06D	AC00	*	*	AC0	PE2D
A05E, A06E	AC01	*	*	AC1	PE2E
A05H, A06H	AC02	*	*	AC2	PE2H
A05K, A06K	AC03	*	*	AC3	PE2K
A05M, A06M	AC04	*	*	AC4	PE2M
A05P, A06P	AC05	*	*	AC5	PE2P
A05S, A06S	AC06	*	*	AC6	PE2S
A05T, A06T	AC07	*	*	AC7	PE2T
A05V, A06V	AC08	*	*	AC8	PE2V
B05D, B06D	AC09	*	*	AC9	PF2D
B05E, B06E	AC10	*	*	AC10	PF2E
B05H, B06H	AC11	*	*	AC11	PF2H

*Note: Collector of Grounded-Emitter Transistor

TABLE I-4

PROGRAMMED INPUT/OUTPUT CONTROL

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B05M, B06M	INTREQ	*1 —◇	*1 —◇	INTERRUPT REQUEST	PF2M
B05K, B06K	SKIP	*1 —◇	*1 —◇	SKIP	PF2K
B01K, B02K	IOP1	—▶	—▶	IOP1	MF34K
B01M, B02M	IOP2	—▶	—▶	IOP2	MF34M
B01P, B02P	IOP4C	—▶	—▶	IOP4	MF34P

*Note: Collector of Grounded-Emitter Transistor

TABLE I-5

DATA-BREAK ADDRESS LINES

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A09H	ADREX3			ADDR EXT 3	ME30H
A09E	ADREX2			ADDR EXT 2	ME30E
A09D	ADREX1			ADDR EXT 1	ME30D
A07D	DADR00			DATA ADDR 0(1)	PE3D
A07E	DADR01			DATA ADDR 1(1)	PE3E
A07H	DADR02			DATA ADDR 2(1)	PE3H
A07K	DADR03			DATA ADDR 3(1)	PE3K
A07M	DADR04			DATA ADDR 4(1)	PE3M
A07P	DADR05			DATA ADDR 5(1)	PE3P
A07S	DADR06			DATA ADDR 6(1)	PE3S
A07T	DADR07			DATA ADDR 7(1)	PE3T
A07V	DADR08			DATA ADDR 8(1)	PE3V
B07D	DADR09			DATA ADDR 9(1)	PF3D
B07E	DADR10			DATA ADDR 10(1)	PF3E
B07H	DADR11			DATA ADDR 11(1)	PF3H

TABLE I-6

DATA-BREAK INPUT LINES

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A08D	DABT00			DATA-BIT 0	PE4D
A08E	DABT01			DATA-BIT 1	PE4E
A08H	DABT02			DATA-BIT 2	PE4H
A08K	DABT03			DATA-BIT 3	PE4K
A08M	DABT04			DATA-BIT 4	PE4M
A08P	DABT05			DATA-BIT 5	PE4P
A08S	DABT06			DATA-BIT 6	PE4S
A08T	DABT07			DATA-BIT 7	PE4T
A08V	DABT08			DATA-BIT 8	PE4V
B08D	DABT09			DATA-BIT 9	PF4D
B08E	DABT10			DATA-BIT 10	PF4E
B08H	DABT11			DATA-BIT 11	PF4H

TABLE I-7

DATA-BREAK CONTROL SIGNALS

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B07K	BKRQ#	*	*	BREAK REQUEST	PF3K
B07M	DICTL			TRANSFER DIRECTION	PF3M
B07P	BBREAK			B BREAK	PF3P
B07S	ADDACC			ADDRESS ACCEPTED	PF3S
B01S, B02S	BT1C			BT1	MF34S
B01T, B02T	BR2A			BT2A	MF34T
B01V, B02V	BPCLRC			B POWER CLEAR	MF34V

*Note: Collector of a Grounded-Emitter Transistor.

PANEL 1 ... COMMON SECTION

	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16	
	W021	W021	W021	W021	W021	W021	W021	W021	W021	R107	R111	R107	R002	R107	R141	R107	
A																	A
B																	B
C												GNDA12			GNDA15		C
D	BAC00	BAC00	BMB00	BMB00	AC00	AC00	DADR00	CABT00	ADREX1	ADREX3	XINT+	BKSL#	BMB03-	BAC00-	TSTSKP	EAC00-	D
E	BAC01	BAC01	BMB01	BMB01	AC01	AC01	DADR01	CABT01	ADREX2	ADDR00		GNDA12	BMB03	BAC00	BAC00-	EAC00	E
F										ADREX2		BPCLK	SELNC	BAC01-	EAC00	EAC01-	F
H	BAC02	BAC02	BMB02	BMB02	AC02	AC02	DADR02	CABT02	ADREX3	ADDR01	INTREQ	BPCLRC	BMB04-	BAC01	BAC01-	EAC01	H
J										ADREX1		IOP4	BMB04	BAC02-	EAC01	EAC02-	J
K	BAC03	BAC03	BMB03-	BMB03-	AC03	AC03	DADR03	CABT03		ADDR02	RINT+	IOP4C	SELNC	BAC02	BAC02-	EAC02	K
L										DADR00		LDAC-	BMB05-	BAC03-	EAC02	EAC03-	L
M	BAC04	BAC04	BMB03	BMB03	AC04	AC04	DADR04	CABT04		ADDR03		LDAC+	BMB05	BAC03	BAC03-	EAC03	M
N										DADR01	INTREQ	CTWD0	SELND	BAC04-	EAC03	EAC04-	N
P	BAC05	BAC05	BMB04-	BMB04-	AC05	AC05	DADR05	CABT05		ADDR04		DEVSL0	BMB06-	BAC04	BAC04-	EAC04	P
R										DADR02	IOP1	CTWD1	BMB06	BAC05-	EAC04	EAC05-	R
S	BAC06	BAC06	BMB04	BMB04	AC06	AC06	DADR06	CABT06		ADDR05	ENBL	DEVSL1	SELND	BAC05	BAC05-	EAC05	S
T	BAC07	BAC07	BMB05-	BMB05-	AC07	AC07	DADR07	CABT07		DADR03		CTWD2		SELDV	EAC05	GRPSEL	T
U										ADDR06	LDAC+	DEVSL2			GNDA15	SELDV	U
V	BAC08	BAC08	BMB05	BMB05	AC08	AC08	DADR08	CABT08			LDAC+			SELND	GNDA15		V

	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16	
	W021	W021	W021	W021	W021	W021	W021	W021	W021MG	R107	R111	R001	R111	R107	R141	R107	
A																	A
B																	B
C															GNDB15		C
D	BAC09	BAC09	BMB06-	BMB06-	AC09	AC09	DADR09	CABT09	ADDR00	DADR04	BMB07	TSTSKP	ICP2	BAC06-	TSTSKP	EAC06-	D
E	BAC10	BAC10	BMB06	BMB06	AC10	AC10	DADR10	CABT10	ADDR01	ADDR07	BMB08	SKIP1	ENBL	BAC06	BAC06-	EAC06	E
F									ADDR02	DADR05	DEVND0	CTWD0	SKIP1	BAC07-	EAC06	EAC07-	F
H	BAC11	BAC11	BMB07-	BMB07-	AC11	AC11	DIAD11	CABT11	ADDR03	ADDR08	DEVSL0	SKIP2	SKIP	BAC07	BAC07-	EAC07	H
J									ADDR04	DADR06	DEVSL0	CTWD0		BAC08-	EAC07	EAC08-	J
K	IOP1	IOP1	BMB07	BMB07	SKIP	SKIP	HKRQ#		ADDR05	ADDR09	BMB07	SKIP3	XINT+	BAC08	BAC08-	EAC08	K
L									ADDR06	DADR07	BMB08-	GRPSEL	ICP1	BAC09-	EAC08	EAC09-	L
M	IOP2	IOP2	BMB08-	BMB08-	INTREQ	INTREQ	DICTL		ADDR07	ADDR10	DEVND1	DEVND0	SKIP2	BAC09	BAC09-	EAC09	M
N									ADDR08	DADR08	DEVSL1	GRPSEL	SKIP	BAC10-	EAC09	EAC10-	N
P	IOP4C	IOP4C	BMB08	BMB08			BBREAK		ADDR09	ADDR11	DEVSL1	DEVND1		BAC10	BAC10-	EAC10	P
R									ADDR10	DADR09	BMBD7-	GRPSEL	RINT+	BAC11-	EAC10	EAC11-	R
S	[illegible]T10	[illegible]T10	BMB09	BMB09			ACCACC		ADDR11	ADDR12	BMB08	DEVND2	ICP2	BAC11	BAC11-	EAC11	S
T	BT24	BT24	BMB10	BMB10					ADDR12	DADR10	DEVND2	DEVSL2	SKIP3	ENBL	EAC11	BACTY	T
U									ADDR13	ADDR13	DEVSL2	ENBLND	SKIP	DEVSL1	GNDB15	BAC09-	U
V	BPCLRC	BPCLRC	BMB11	BMB11							DEVSL2			ENBLND	GNDB15		V

TABLE I-8.

PANEL 1 ... COMMON SECTION

	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32	
	R123	R202		R123								W050S					
A																	A
B																	B
C																	C
D	EAC00-	IOP4		#SR00+								#XMT+					D
E	EAC01-	DEVSLC		#SR01+								#REC+					E
F	LDAC-	BPCLR										#SRSV+					F
H	AC00			CABT00								#DLST+					H
J	AC01	XINT+		CABT01								#PAR+					J
K	EAC02-	#SRSV-		#SRC2+								#EBPC+					K
L	EAC03-	#XMT-		#SRC3+								#IFMD+					L
M	LDAC-											#STRDY					M
N	AC02	IOP4		DABTC2								#TMRD+					N
P	AC03	DEVSLC		DABT03								#RING					P
R	EAC04-	BPCLR		#SRC4+								#CARDT					R
S	EAC05-			#SRC5+													S
T	LDAC-	RINT+															T
U	AC04	#SRSV-		DABT04													U
V	AC05	#REC-		CABT05													V

	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32	
	R123	W002	R111	R123													
A																	A
B																	B
C																	C
D	EAC06-	EAC00	IOP4C	#SRC6+													D
E	EAC07-	EAC01	CTWDC	#SRC7+													E
F	LDAC-	EAC02															F
H	AC06	EAC03	#SRSV+	DABT06													H
J	AC07	EAC04		CABT07													J
K	EAC08-	EAC05	BT1C	#SRC8+													K
L	EAC09-	EAC06		#SRC9+													L
M	LDAC-	EAC07															M
N	AC08	EAC08	BT1	DABT08													N
P	AC09	EAC09	BT1	DABT09													P
R	EAC10-	EAC10		#SR10+													R
S	EAC11-	EAC11		#SR11+													S
T	LDAC-	DIAC11															T
U	AC10	DICTL		DABT10													U
V	AC11			DABT11													V

TABLE I-9

PANEL 2 ... PORT O/LINE ADAPTOR 1

	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16	
	#2?1C	EIAR	R111	W521	R111	R001	R302	R111	R201	R205	R205	R205	R2C5	R205	R201	R205	
A																	A
B																	B
C		#GND02		#GND24			#GND06									#GND14	C
D	#SD3	#GND02	#RD+	#SRCK	#SCPF+	#REC-		#RECE-		#SHIFT	#SHIFT	#SHIFT	#SHIFT	#SHIFT		#SHIFT	D
E	#RDA	#RINGE	#PEC+		#LINE+	#DTND1	#PQSC+		#SHIFT	#SR01-	#SR03-	#SR05-	#SR07-	#SR09-	#SHIFT	#SDBF+	E
F	#RSB			#SRCK	#CTS?I	#REC-	#GND06		#RD+	#ZERSR	#ZERSR	#ZERSR	#ZERSR	#ZERSR	#SR10+		F
H	#CSDB	#RING	#RC-		#CLT1	#DTND2		#REC+		BMB01	BMB03	BMB05	BMB07	BMB09		#GND14	H
J	#SRDB	#RING	#RD-		#CLT1	#REC-	#A06JK			#SR01+	#SR03+	#SR05+	#SR07+	#SR09+			J
K	#TRDY?	#GND02			#PTBF+	#RSND	#AC6JK	#XMTE-	#ZRCSR	#SR00-	#SR02-	#SR04-	#SR06-	#SR08-	#ZERSR	#SR11+	K
L	#RINGP	#CSCB		#GND04	#LINE-				#SR00+	#SR00+	#SR02+	#SR04+	#SR06+	#SR08+	#SR11+	#SR11-	L
M	#CDETP	#DELAY		#L04	#CTND2		#BFIX		#SR00-	#MBSR	#MBSR	#MBSR	#MBSR	#MBSR	#SR11-	#FRZE	M
N		#CS+		#L04	#CLT1		#IFMD+	#XMT+		#SHIFT	#SHIFT	#SHIFT	#SHIFT	#SHIFT		#SHIFT	N
P	#SCTB	#CS+					#REC-		#SHIFT	#SR02+	#SR04+	#SR06+	#SR08+	#SR10+	#SHIFT	#PATY+	P
R	#SCRB	#GND02	#BFIX	#SCRB	#XMT-				#RD-	#SR02-	#SR04-	#SR06-	#SR08-	#SR10-	#SR10-	#PATY-	R
S		#SRCB			#XTFC+		#A06ST		#MBSR	BMB02	BMB04	BMB06	BMB08	BMB10	#MBSR	#GND14	S
T					#RSND		#AC6ST		BMB00	#SR01-	#SR03-	#SR05-	#SR07-	#SR09-	BMB11	#EP2	T
U		#STRLY	#DELAY		#RS1					#SR01+	#SR03+	#SR05+	#SR07+	#SR09+		#EP2	U
V		#STRDY			#RS1		#PRI			#MBSR	#MBSR	#MBSR	#MBSR	#MBSR		#ZROSR	V

	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16	
	#502	EIAR		W521	W501	R202	R602	R602	R602	R602	R202	R107	R. 7	R121	R111	R002	
A																	A
B																	B
C		#GND34		#GND36							#GND43		BKSLB				C
D	#DUTI	#GND34		#SCK	#CCTD		#JMP39	#JMP40	#JMP41		#SRSV+	#CARDT	#BRENB	#IOPCS	#ENDI	#SR00-	D
E		#PDB			#CCT			#FR3+			#RSYN-	#CDTD	#BRI	#EBPC+	#BRENB	#SR01-	E
F	#SDB			#SCK	#CCTD	#PWCLR		#EXMT			#PWCLR	#DY+	BKRQ#	#DTSY+		#DSYND	F
H	#?CSD+	#RCBI				#REG-	#CLOCK	#BRKON		#CLOCK	#RSYN-	#DY-	#BKRC+	#F1	#CHRDN	#SR02-	H
J		#RDBI				#RFC+	#DTSY-	#ENZR		#SYNC-		#STCK	#ENAX+	#IFMD-	#CHRDN	#SR03+	J
K	#?SB	#GND34			#L37	#SRCK	#ZERSR	#ZRCSR	#PWCLR	#START	#SRSV-	#SCK	#ENAX-	#DTSY-	#IFMC-	#DSYND	K
L	#TM?	#CDETB		#GND35	#U37	#RECE-	#ZROSR	#START	BPCLR		#REC-	#RD+	#ENBL>	#ESFT	#REC+	#SR04-	L
M				#L36	#L37		#JMP39	#JMP40	#JMP4I			#RDBI	#ENBL-	#DY-	#DSYND	#SRC5+	M
N	#TRDYP	#CDT		#L36	#L37						#START	#DTSY+	#ENDI	#SVC-	#DTSY-	#DSYND	N
P	#V+?01	#CDT					#STCK				#GND43	#DTSY-	#END	#IOPCS	#DTSY-	#SR06+	P
R	#J-?01			#SCTB	#JM37	#PWCLR	#XMT-				#PWCLR	#CS-		#EFRO		#SR07-	R
S	#V+B01				#CCT	#XMT-	#SRCK	#CLOCK	#BRKON		#SYNC-	#CS+		#F1		#DSYND	S
T					#JP27	#XMT+	#REC-	#ESFT	#EXMT				#BLOCK	#SVC-			T
U						#STCK	#CLOCK	#SHIFT	#MBSR	#END	#CLCCK		BKSLB	#ICPCS			U
V	#V-?01					#XMTE-				#FR3+	#SVC-				#ENDI		V

TABLE I-10.

PANEL 2 ... PORT 2/LINE ADAPTER 1

	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32	
	R202			R201	R201	R201	R205	R205	R205	R205	R123	R123		R123			
A																	A
B																	B
C					#GND19	#GND20											C
D	#FR3+						#INVMK	#INVMK	#STCK	#BPKDN	#SRSV+	#EBPC+		#CFR3+			D
E	#DY-			#INVMK	#ALAC	#START			#CLSD-	#RQSD-	#DLST+	#IFMD+		#CFR2+			E
F				BACC7	#GND19	#GND20	#PWCLR	#PWCLR	#PWCLR	#PWCLR	#ENBL+	#ENBL+		#ENAX+			F
H	#LINE-			#REC-				#PAR1		#RS1	EAC00	EAC06		EAC08			H
J	#LINE+			#XMT+			#EBPC+	#PAR+	#CLSD+	#RQSD+	EAC01	EAC07		EAC09			J
K	#CLOCK			#PWCLR	#PWCLR	#PWCLR	BAC06	EAC02	#CS-	#XTRQ-	#PAR+	#STRCY		#CFR1+			K
L	#LINE+			#IFMD+	#PKRQ+		BAC06	BAC02	#CS+	#XTRQ+	#RQSD+	#TMRD+		#CFR0+			L
M	#FRZE			#IFMD-		#SVC-		#CLOCK		BT1	#ENBL+	#ENBL+		#ENAX+			M
N	#FR3+					#RSTRT	#INVMK	#INVMK	#INVMK	#INVMK	EAC02	EAC08		EAC10			N
P	#PATY-			#INVMK	#FR3+	#REC-	#TMRD+	#DLST+	#SRSV+	#XTRQ+	EAC03	EAC09		EAC11			P
R				BAC07	#IFMD-	#XMT+			#SRSV-	#XTRQ-	#XTRQ+	#RING		#RQSD+			R
S	#PTBF+			#CLOCK	#START	#XMT-		#SRSV-	#ESRSV		#CLSD+	#CARDT		#RQSD+			S
T				#DTSY-	#XMT-	#REC+	BACTY	BAC01	BAC00	BAC04	#ENBL+	#ENBL+		BKSL#			T
U	#FR3+			#XMI-			BACTY	EAC01	BAC00	BAC04	EAC04	EAC10		DIAD11			U
V	#PATY+			#REC+				#CHRDN	#CHRDN		EAC05	EAC11		CICTL			V

	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32	
			R001	R111	R121	R121	R121	R001	R111	R603	R602	R205	R205	R205	R205		
A																	A
B																	B
C											#GND59	#GND60	#GND61				C
D			#TMRD+	#RQSD+		#EP2		CTWD1		IOP4	#JMP59	#CLOCK	#FR1+	#LDAUX	#LDAUX		D
E			#XMTNL	#CLSD+		#RD+		#BLND		#ENBL-				#CFR0-	#CFR2-		E
F			#CARDT	#XMTND		#DTSY+		#BLOCK	#BLND	#INVMK		#FRZE	#FRZE	#PWCLR	#PWCLR		F
H			#XMTND	#XMTL-	#ENZR	#EP2	#ADAC	#BLND	#ENBL-		#SVC-	#CFR0-	#CFR2				H
J			#STRCY	#XMTL-	#REC+	#SR11+	ACDACC	CTWD2	#ENBL-		#GND59	#FR0+	#FR2+	#CFR0+	#CFR2+		J
K			#XMTND	#FR3+	#IFMD+	#XMT+	BKSL#	#AXND		#ZROSR	#FRZE	#EFR0	#GND61	BAC11	BAC09		K
L			#FR2+	#FR3+	#EXMI	#EP2	#BRKDN	#BLOCK		#XTRQ+	#PWCLR	#EFR0	#GND61	BAC11	BAC09		L
M			#DYNC	#DYNC	#IFML+	#RD+	BKSL#	#AXNC	#AXND	#LDFR	#JMP59	#LDFR	#LDFR				M
N			#FR1+	#DY-	#XTRQ+	#REC+	BBREAK	#REC+	#ENAX-			#FR0+	#FR2+	#LDAUX	#LDAUX		N
P			#DYNC	#DY-	#XMT+	#IFMD+	BT1C	#PARND	#ENAX-	#MBSR	#IFMD-	#FR1+	#FR3+	#CFR1+	#CFR3+		P
R			#LAPC+	#REC+	#RECE-	#ESRSV	#PAR1	#DY+	#RD+	IOP4	#XMT-			#CFR1-	#CFR3-		R
S			#DYNC	#IFMD+	#RQSD-	#XMT+	#RD-	#PARND	#PATY-	#ENAX-	#IFMD+	#CFR1-	#CFR3-				S
T			#IFMD+		#CLSD-	#XTRQ+	#REC+		#PARND	#LDAUX	#REC-	#GND60	#GND61	BAC10	BAC08		T
U			#DYNC	#ESRSV	#CARLT	#IFMD+	#DY+		#PAR1		#RSTRT	#GND60	#GND61	BAC10	BAC08		U
V					#STRCY		#PATY+					#LDFR	#LDFR				V

TABLE I-11.

APPENDIX II

201A LINE ADAPTOR INTERFACE FOR USE ON THE DATA CONCENTRATOR

APPENDIX II

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201A LINE ADAPTOR INTERFACE
FOR USE ON
THE DATA CONCENTRATOR

The remainder of the logic and details of the 201A communication adaptors used on the Data Concentrator are presented in this Appendix. Figure II-1 shows in block form the general organization of the Data Concentrator, to the extent that it concerns the 201A line adaptors. The control of AC transfers and interrupts for the PDP-8 is handled by the scanner. In order to address a line adaptor (for the purposes here, a 201A line adaptor) the scan address register must be loaded with what corresponds to the line adaptor's logical address. This logical address, in reality, is the core address of its receive or transmit buffer. When the scanner is interrupted by a line adaptor, it in turn interrupts the PDP-8 with the scan address register set to the receive or transmit buffer address depending on the type of interrupt. The IOT structure is the same as described for the basic 201A line adaptor once the scan address register is pointed to the line adaptor.

The normal operation for the scanner is to scan, in turn, each of the 64 full-duplex lines looking for an interrupt. When an interrupt is found, the scanner is stopped and a PDP-8 interrupt is generated. After servicing the scanner interrupt (indirectly a line adaptor interrupt), the scanner is restarted.

The multiplexor is a buss-type multiplexor where the device presently selected gates its address and data information onto common busses. A device requests a data-break cycle by pulling to ground its break request line, and the data break is granted when its select line goes to -3v. In order to realize this buss concept, certain of the normal PDP-8 signals are electrically inverted at the multiplexor interface.

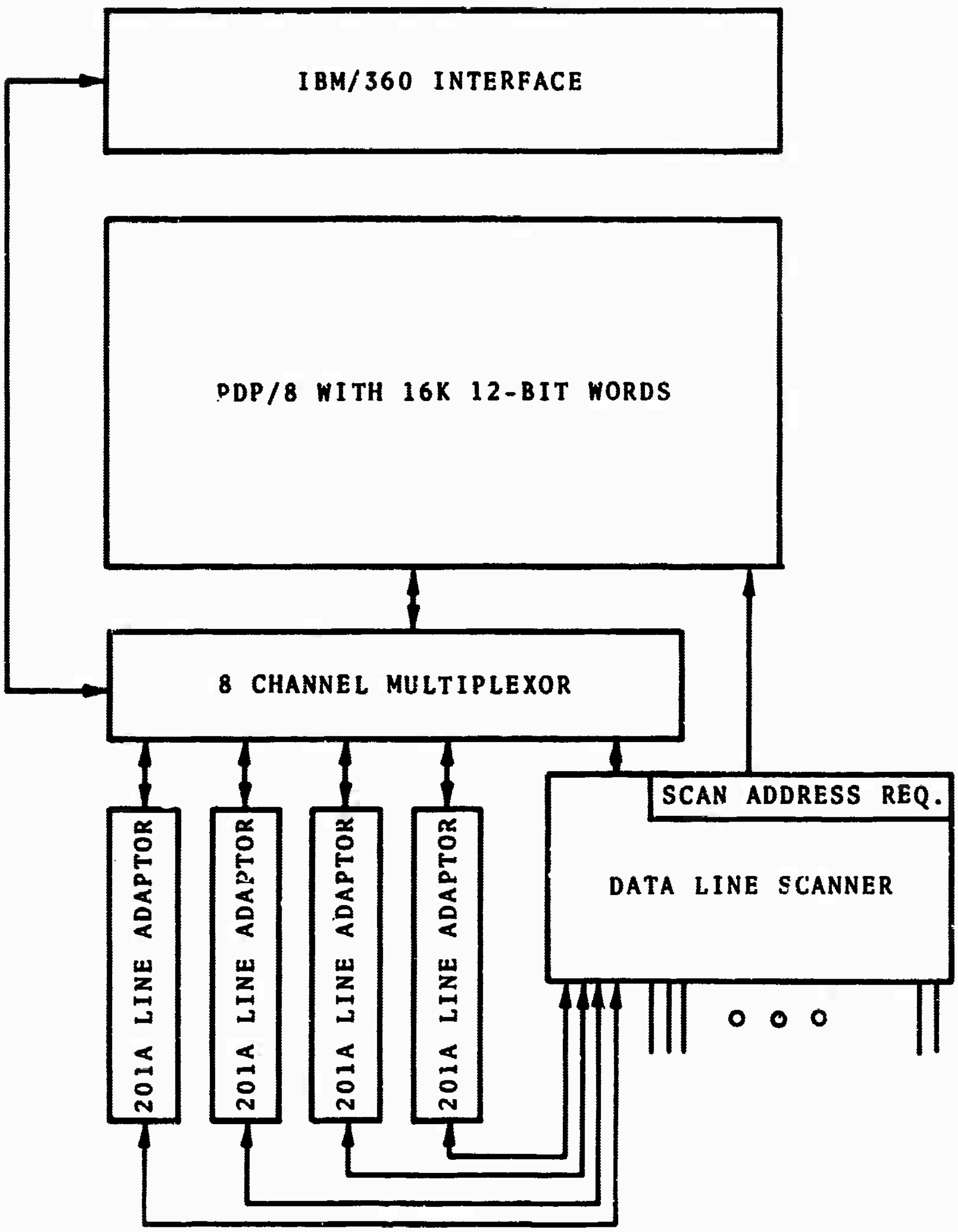


Figure II-1. ORGANIZATION OF THE DATA CONCENTRATOR

There are four 201A line adaptors on the Data Concentrator. They all have a common control section which, in the context of Figure 1, is the PDP-8/201A line adaptor interface. The common section is Bay 1 of the complex with Bays 2-5, representing the four 201A line adaptors. The individual signal names in the 201A line adaptor contain a # sign which is replaced by a 1, 2, 3, or 4 in the particular line adaptor. The common signals are distinguished by the absence of a # sign. Unless otherwise noted, the logic shown in the diagrams in this Appendix is realized in Bay 1.

<u>Data-Break Control</u> (Diagram II-1)

By setting the #BKRQ flip-flop, the line adaptor signals the PDP-8 (through the multiplexor) that a data transfer is desired to or from PDP-8 core. The multiplexor responds with the BKAC# signal when the data-break cycle is granted. The direction of the transfer is specified by the DICTL signal. When the PDP-8 enters the break state, the address is loaded into the memory address register and an address accepted pulse is generated by the PDP-8. At this time, the break request signal must be dropped by the interface. During the break state, as indicated by the logical—and of BBREAK and BKSL#, the BT1 pulse is used to generate a #BRKDN pulse which strobes the contents of the designated memory location from the buffered memory buffer register into the SDR register. The PDP-8 will also strobe the data-break input lines (DABT) into memory at this time in the case that the transfer direction is into core. The break request signal is generated each time the frame counter overflows when in the text state, and when the interface first enters the transmit state to fetch the first character to be transmitted. All of the logic shown in Diagram II-1 is in the individual line adaptor bay.

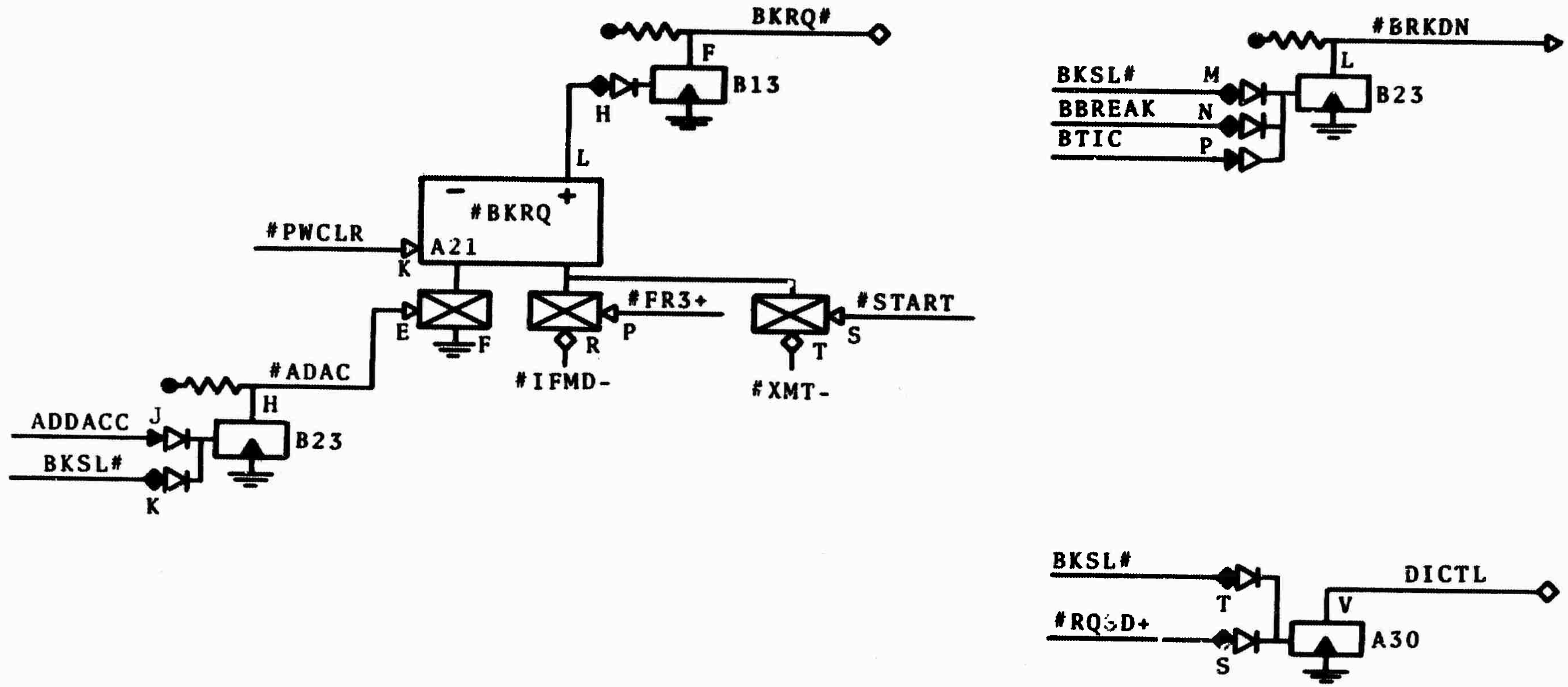


Diagram II-1. DATA-BREAK CONTROL

<u>Data-Break Address and Data Gating</u> (Diagram II-2)

Each 201A line adaptor has assigned two sequential locations in PDP-8 core to be used as buffers for incoming (received) and outgoing (transmitted) data. The low-order four bits, except for the lowest order bit, are specified by an address card shown in Diagram II-5. The high-order five bits (page address) are specified by the Scanner and are gated onto the data address lines when the PGENB signal is given, as derived in Diagram II-3. The remainder of the address bits are specified in Diagram II-3.

The contents of the SDR register are gated onto the data break input lines when the BKSL# signal is present, as shown in Diagram II-2. All of the logic shown in Diagram II-2 is in the individual line adaptor bay.

<u>Common Data Address Gating</u> (Diagram II-3)

There are a total of 128 scanner data lines (64 full-duplex pairs). This corresponds to one full PDP-8 page of buffers. In the twelve-bit PDP-8 address, the high-order five bits specify the page; the low-order bit specifies whether the address is a receive or transmit buffer as the bit is respectively zero or one. The remaining six bits specify which of the 64 line pairs is being referenced. These 64 line pairs are further broken down into eight blocks of eight lines each. Positions 5, 6, and 7 in the address thus specify the block address. A separate cable connects the scanner to each block of line adaptors and in turn provides the block address for those line adaptors, and a common buss (PGENB) to tell the scanner to load the page address on to the data address lines. Diagram II-3 indicates the gating necessary to gate the block address onto the data address lines and pull down the PGENB buss.

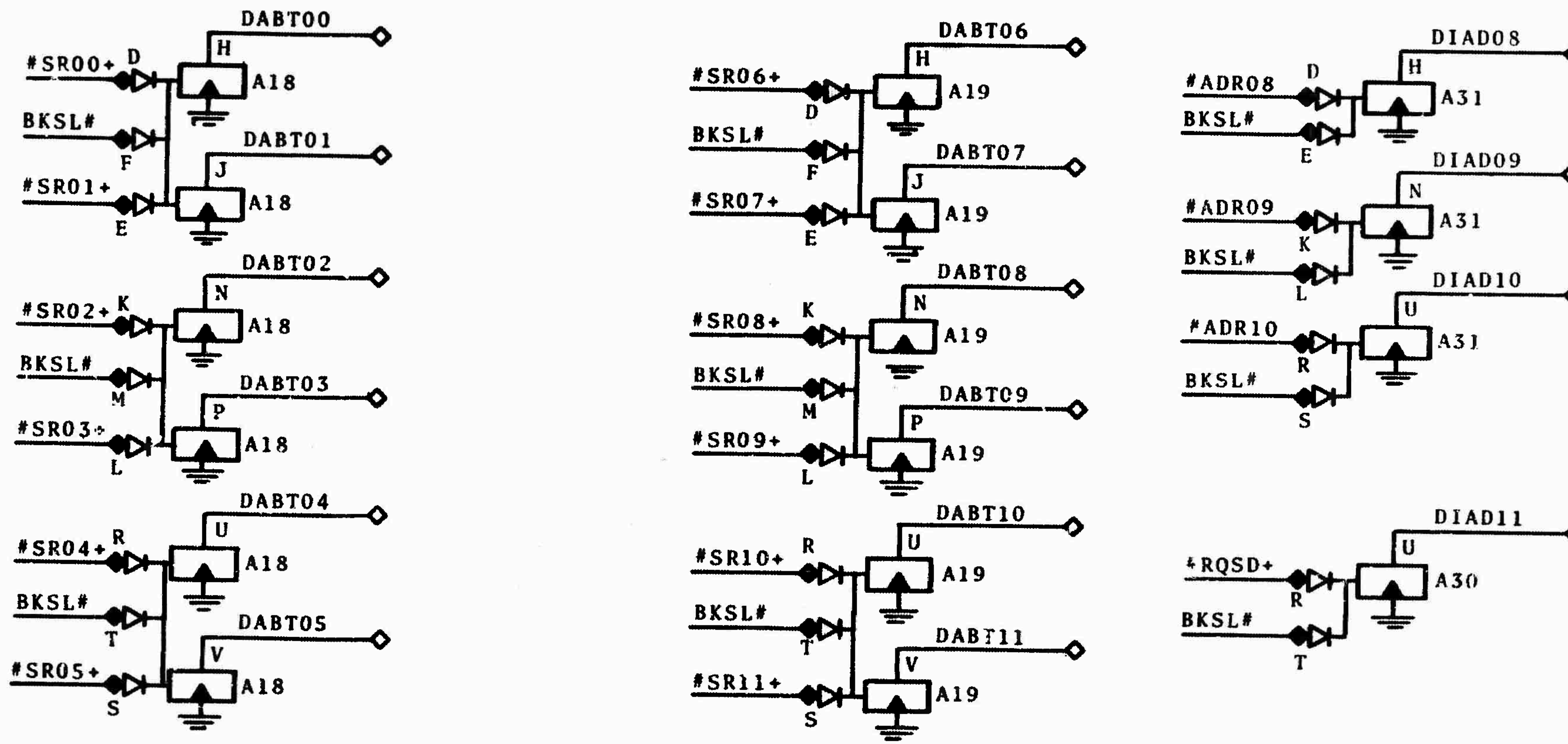


Diagram II-2. DATA BREAK ADDRESS AND DATA GATING

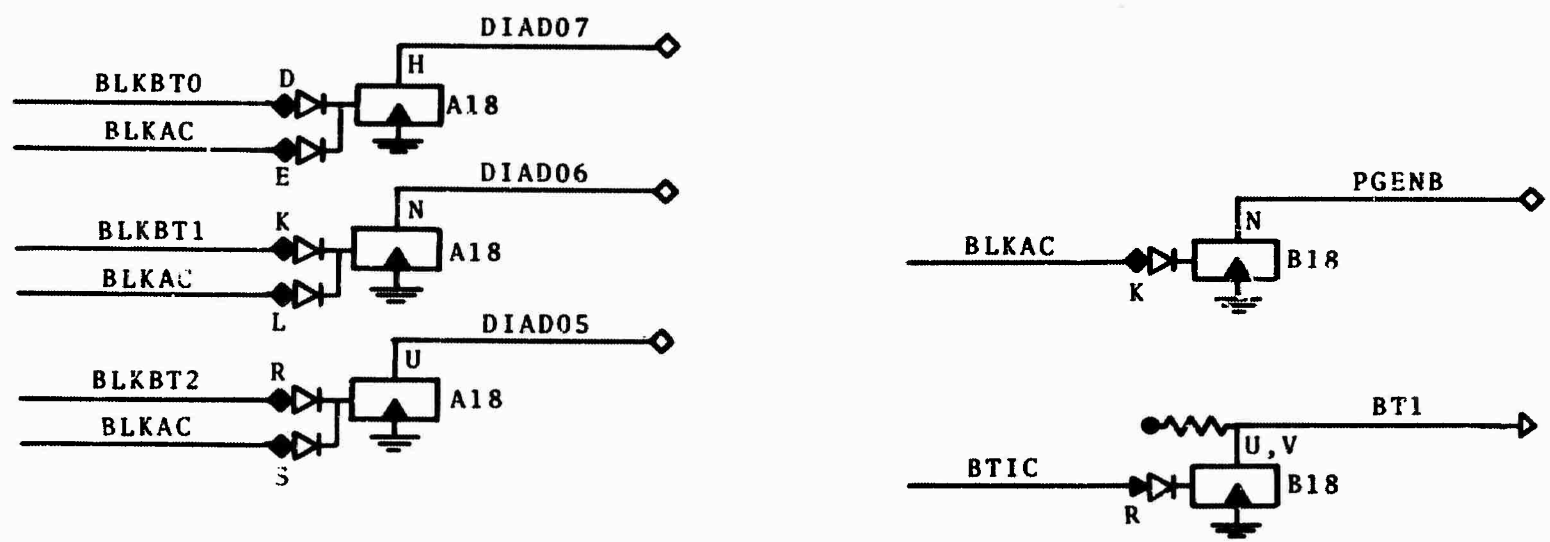


Diagram II-3. COMMON DATA ADDRESS GATING

Scan Address Buffers (Diagram II-4)

These buffers provide the required isolation and signal levels to allow each 201A line adaptor to ascertain whether the current scan address is actually its address. These signals are fed to an address card which decodes the scan address actually assigned to the line adaptor.

Address Decoding (Diagram II-5)

This address card, located in the individual line adaptor bay, provides the line adaptor with its data break address within a scan block and the signals to determine if the current scan address is the line adaptor address.

Data-Break and Device Selection (Diagram II-6)

The first set of gates in Diagram II-6 derives the individual BKSL# signals from the multiplexor signals BKAC#. The BLKAC signal goes to -3v if any of the four 201A line adaptors is granted a data-break cycle by the multiplexor. The signals CTWD1 and CTWD2 are the assertion that the device codes corresponding to Control Word 1 or Control Word 2, respectively, have been detected during an IOT microinstruction.

Device Selection Gating (Diagram II-7)

The gates shown in Diagram II-7 are located in the individual line adaptor bays and provide the signals to differentiate between Control Word 1 and Control Word 2 operations.

Scan Interrupt Service Request (Diagram II-8)

Every time a character is transferred between a 201A line adaptor and the PDP-8's memory, it's character service flag (#SRSV) is set, as described previously. The SCNSVC buss is pulled to ground the next time the scan address matches the

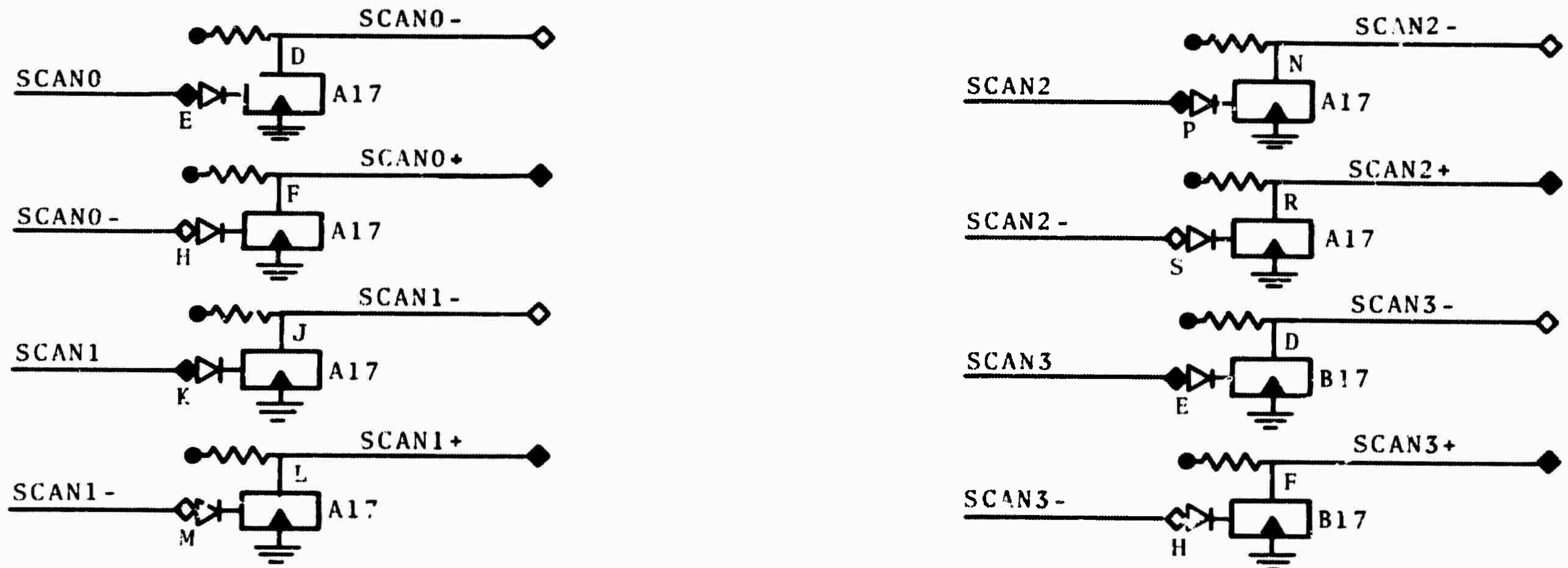
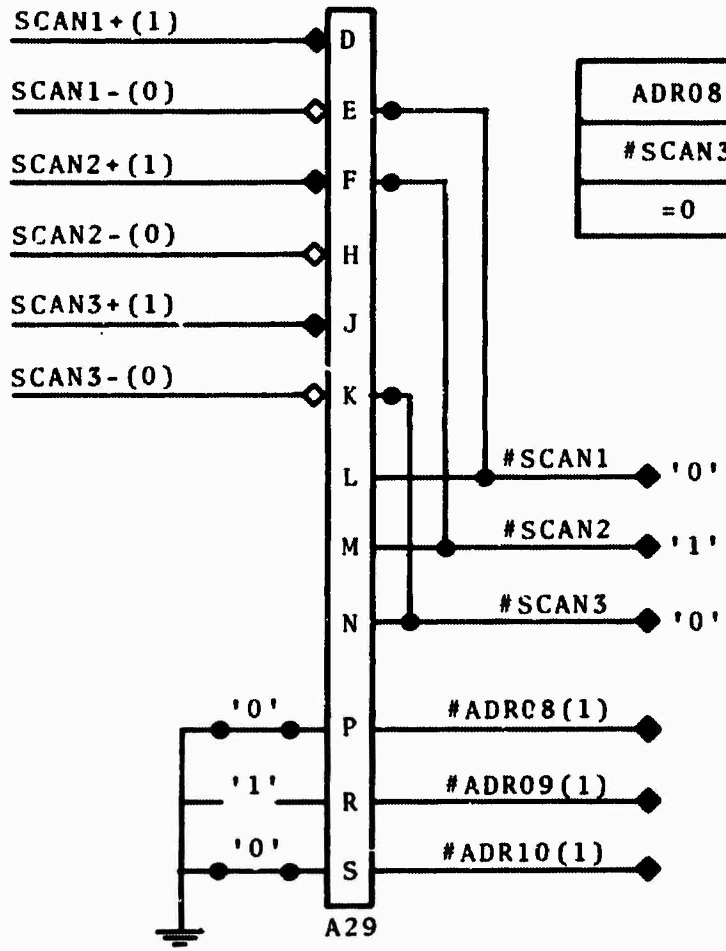


Diagram II-4. SCAN ADDRESS BUFFERS



ADR08	ADR09	ADR10	ADR11
#SCAN3	SCAN2	SCAN1	SCAN0
=0			XMT/REC

SCAN0=1 XMT
SCAN0=0 REC

NOTE: JUMPERS ARE FOR LINE ADAPTOR #2, THUS '#' = '2'

Diagram II-5. ADDRESS DECODING

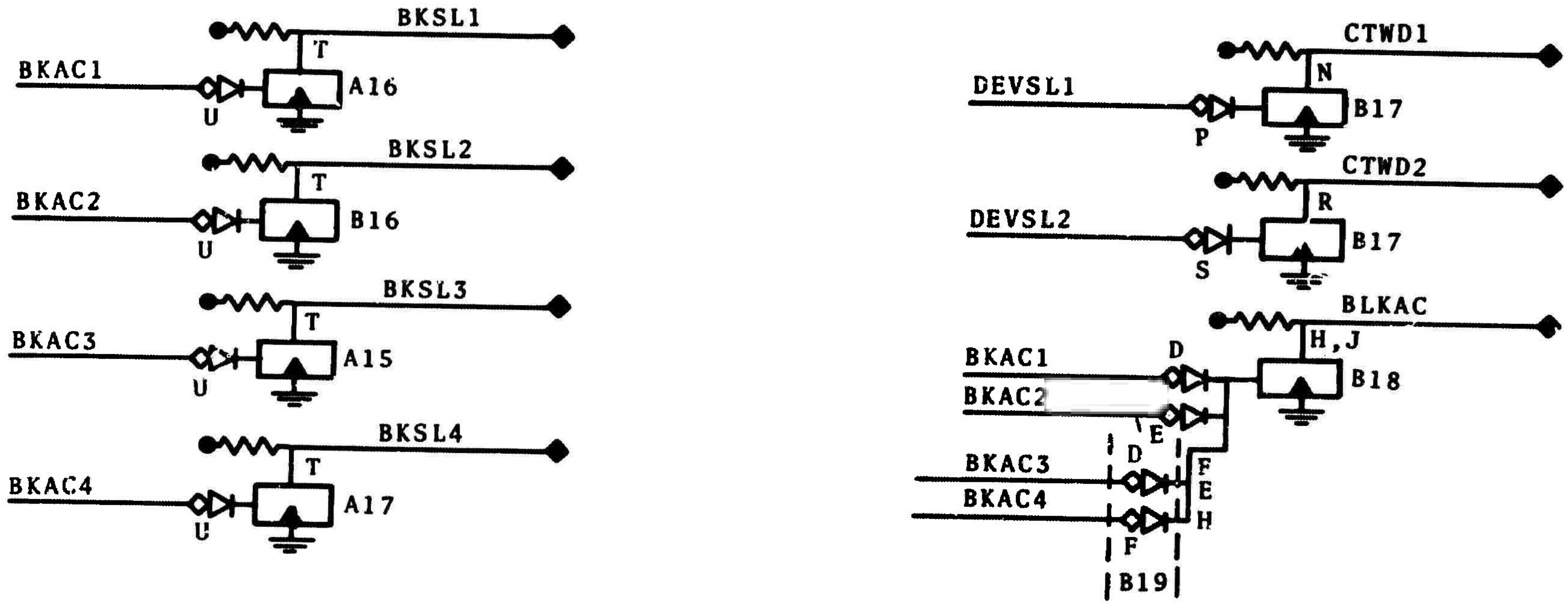


Diagram II-6. DATA-BREAK AND DEVICE SELECTION

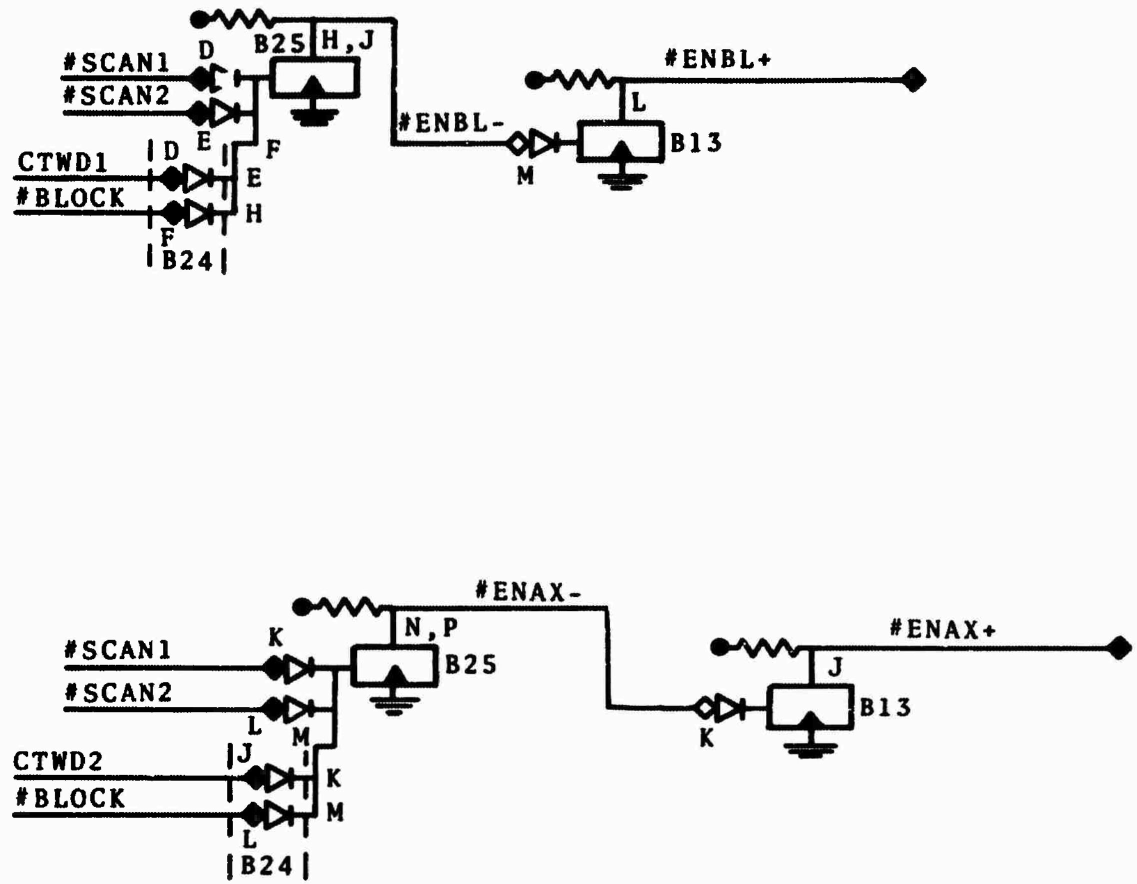


Diagram II-7. DEVICE SELECTION GATING

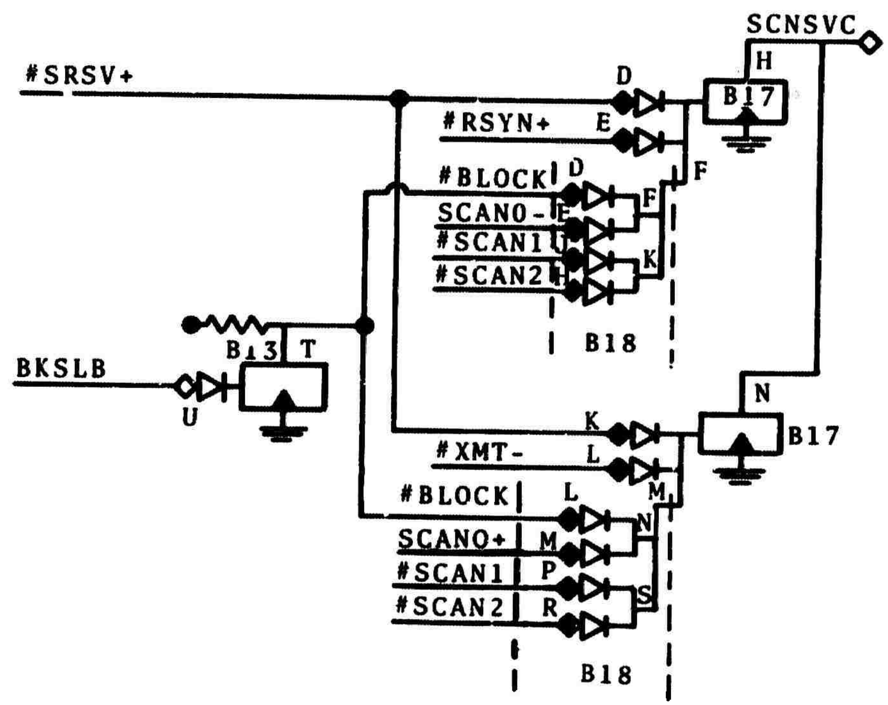


Diagram II-8. SCAN INTERRUPT SERVICE REQUEST

line adaptor's address, as specified by #BlOCK, #SCAN2, #SCAN1, #SCAN0+ . SCNSVC at this time causes a PDP-8 interrupt which the program can then identify.

Transmit Clock Gating (Diagram II-9)

The 201A data sets for the Data Concentrator have externally supplied transmit clocks. This specification allows transmit interrupt staggering and the use of different clock rates. The actual clock selection is made via a jumper card in Bay 1 while the driver for the data set is in the individual line adaptor bay.

"I'm Here" Indication (Diagram II-10)

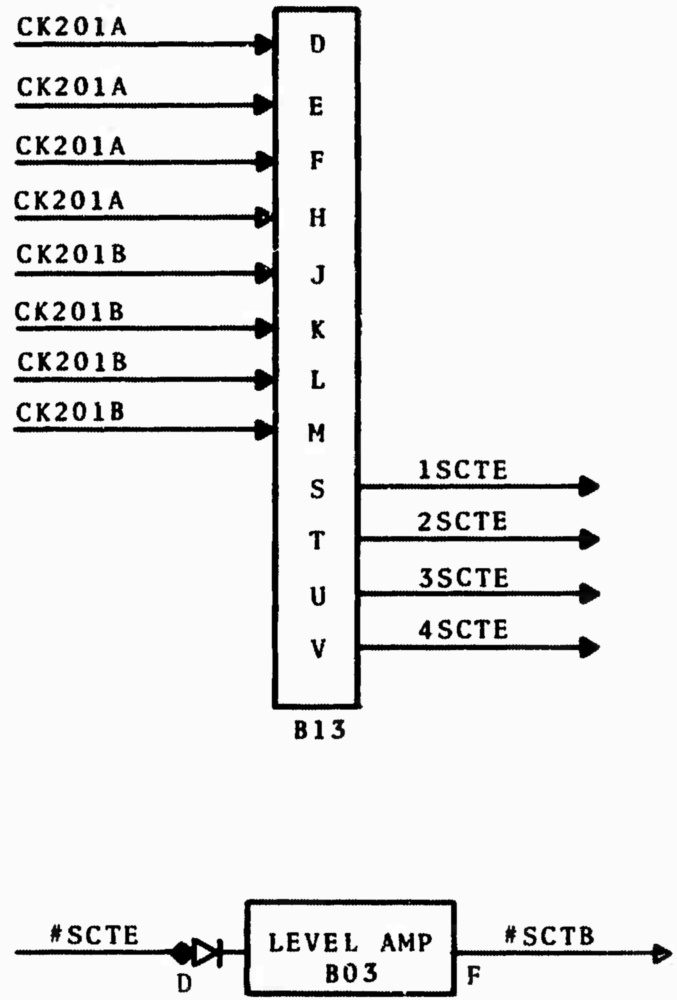
The gating in Diagram II-10, located in the individual line adaptor bays, provides to the scanner a "not here" or "off-line" indication through the #HERE signal.

Buffered Memory Buffer Buffers (Diagram II-11)

This set of buffers is needed for loading reasons in each block of line adaptors. The buffers also provide the necessary inversion to give the correct signal polarity as needed in the line adaptors.

Accumulator Output Buffers (Diagram II-12)

This set of buffers is needed to provide the necessary driving capabilities for the line adaptors. The buffers also provide the necessary inversion to give the correct signal polarity to the line adaptors.



NOTE: JUMPER FROM DESIRED CLOCK TO #SCTE

Diagram II-9. TRANSMIT CLOCK GATING

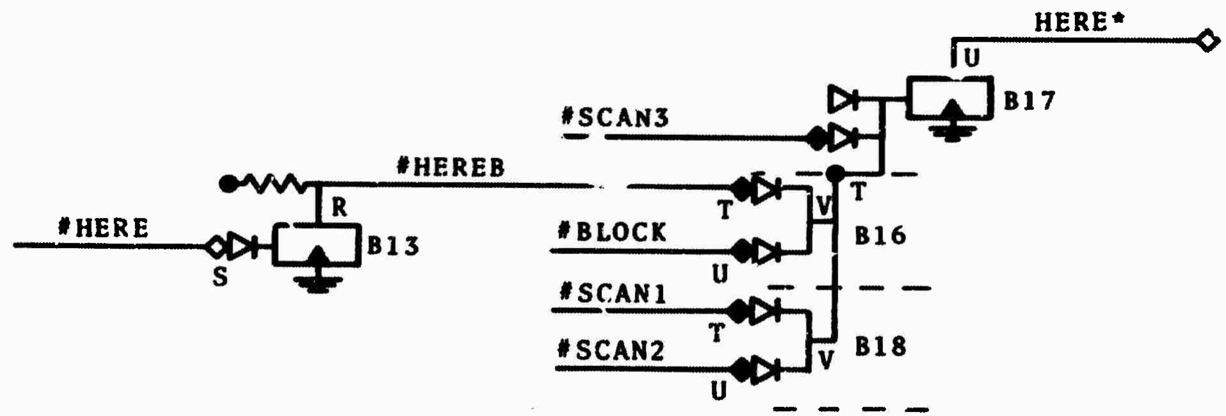


Diagram II-10. 'I'M HERE' INDICATION

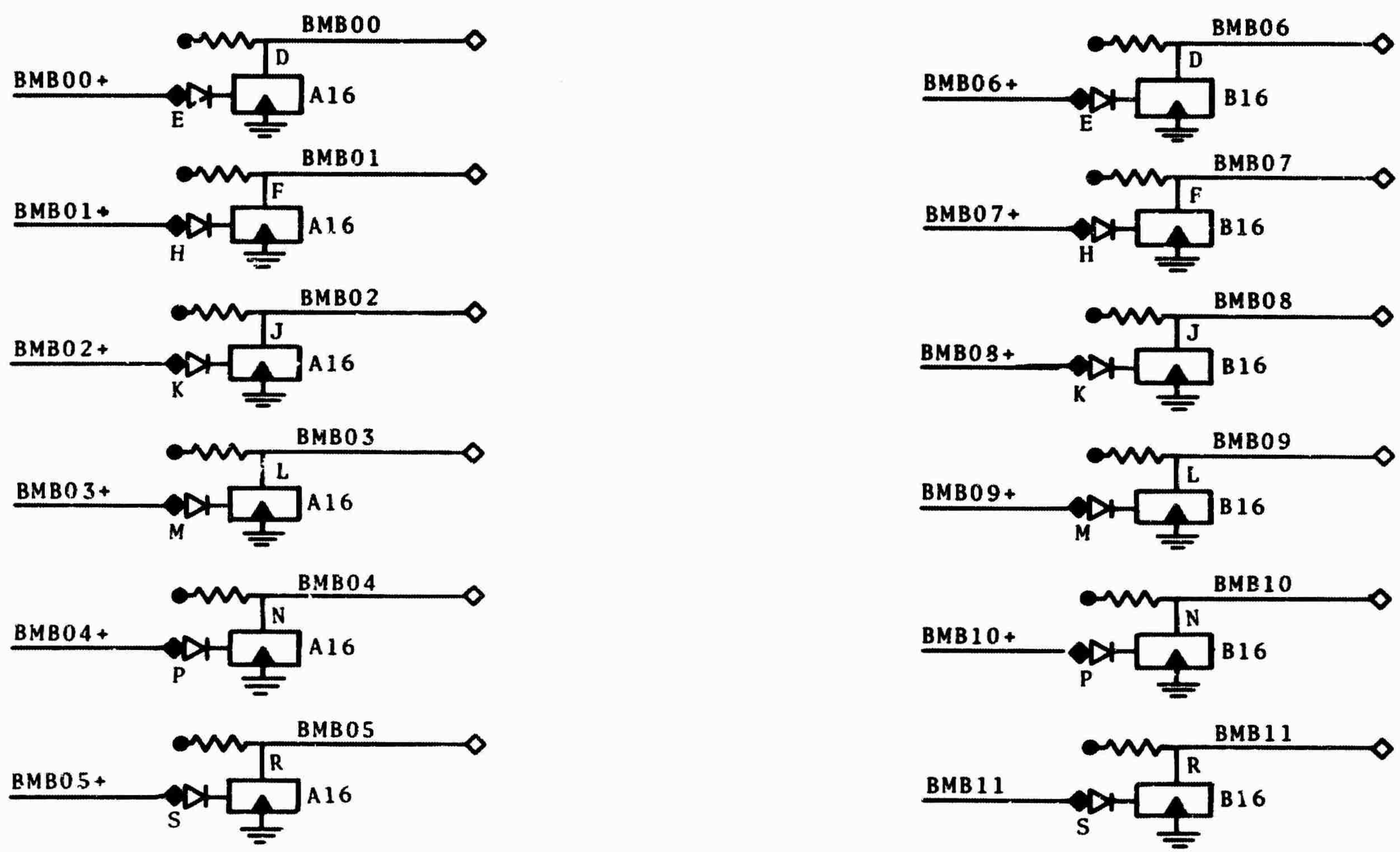


Diagram II-11. BUFFERED MEMORY BUFFER BUFFERS

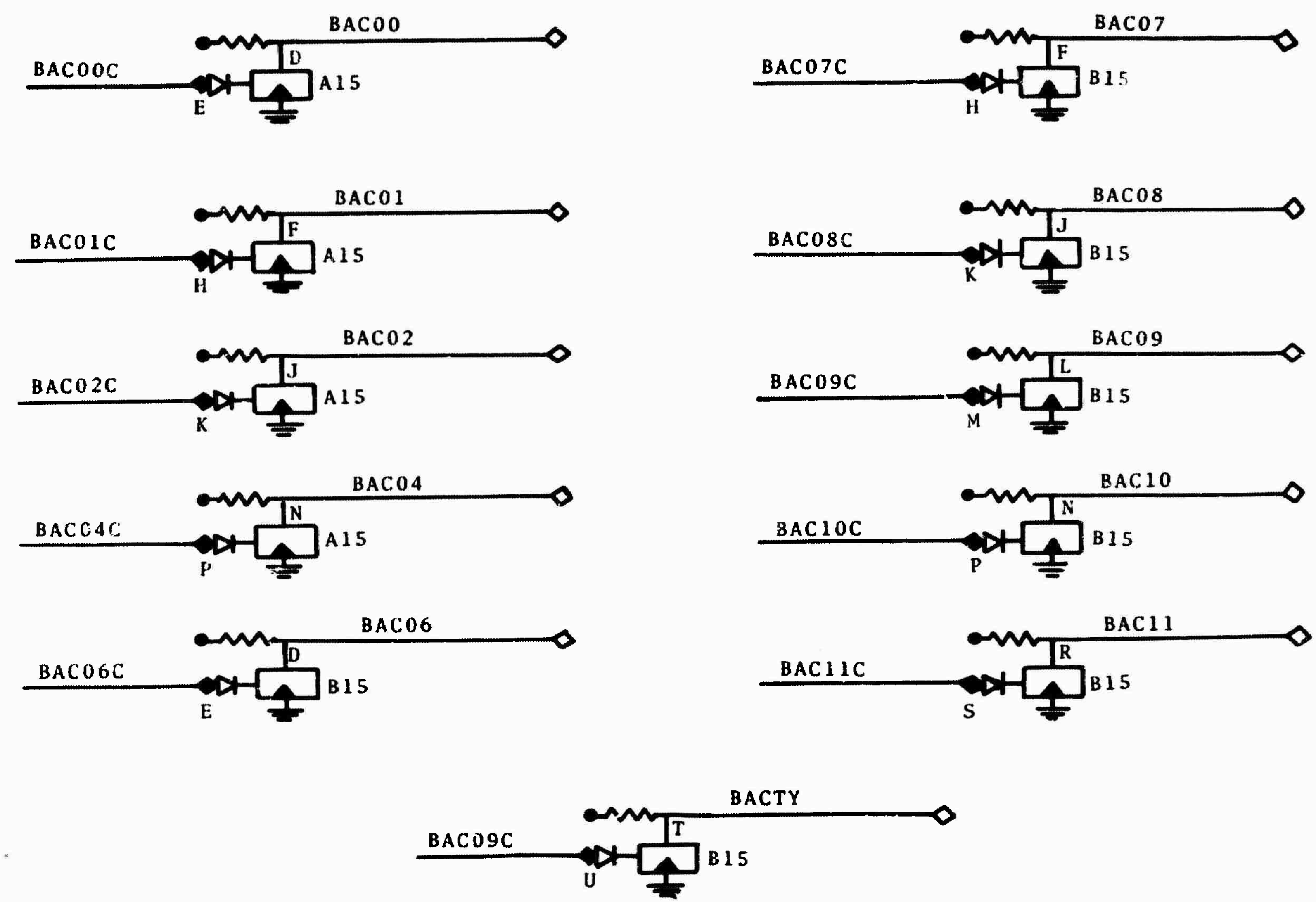


Diagram II-12. ACCUMULATOR OUTPUT BUFFERS

Miscellaneous Circuits (Diagram II-13)

PRYREQ and SPSVC identify to the scanner that the interrupt (SCNSVC) is from a 201A line adaptor. The DTALST buss is used to indicate to the scanner that a line adaptor has a data lost condition (this gate is in the individual line adaptor). The remaining gates provide the necessary electrical signal inversion.

Cable Layout (Diagram II-14)

The input/output cables for the 201A line adaptors are shown in Diagram II-14. The correspondences between the signal names, module positions, and pin connections for the 201A line adaptor block and the multiplexor or scanner are given in Tables II-1 through II-9.

Module Utilizations (Tables II-10 through II-21)

Tables II-10 through II-21 give the module utilization for the four 201A line adaptors comprising the block on the Data Concentrator. In addition to the module utilization, a complete signal name map is also shown.

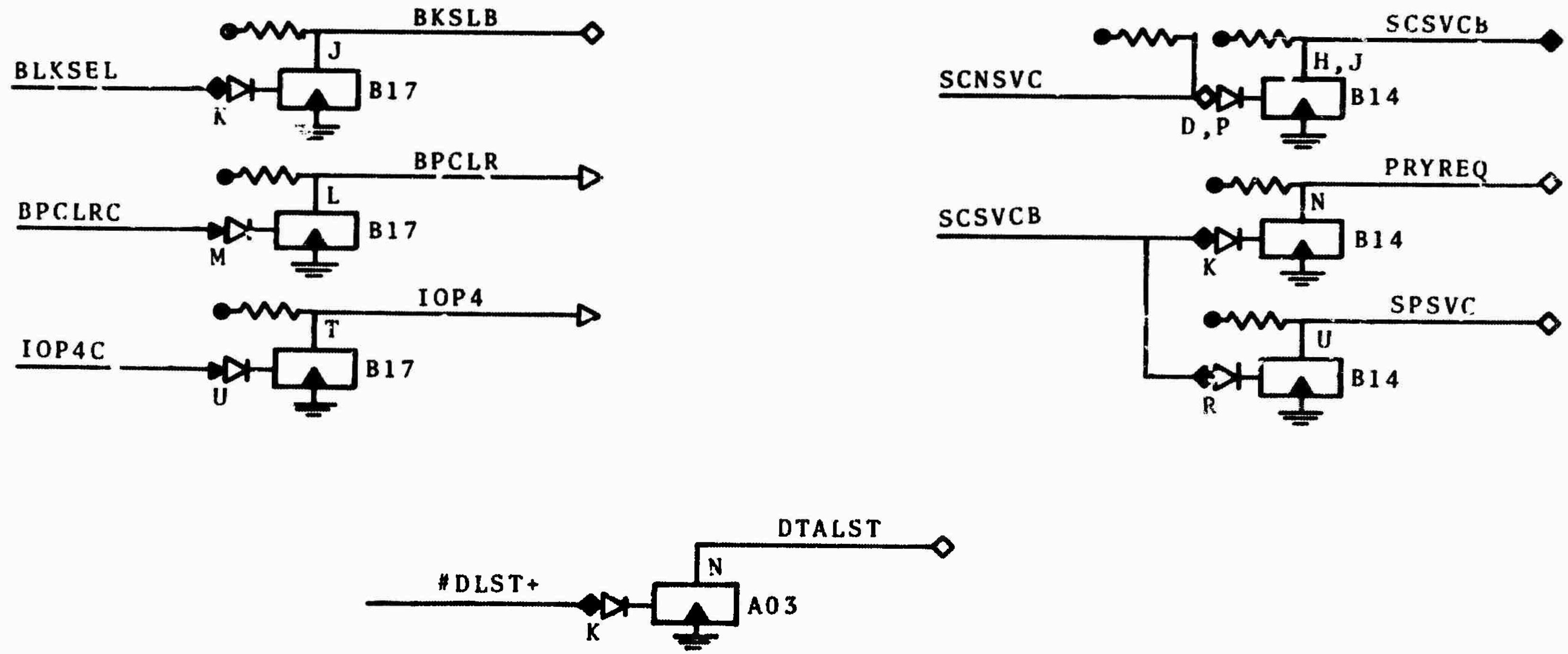


Diagram II-13. MISCELLANEOUS CIRCUITS

'A'

	01 02	03 04	05 06	07 08	09 10	11 12	13 14
D	BAC00C	BMB00+	DIAD00	DABT00	EAC00	SCAN0	--
E	BAC01C	BMB01+	DIAD01	DABT01	EAC01	SCAN1	--
F							
H	BAC02C	BMB02+	DIAD02	DABT02	EAC02	SCAN2	--
J							
K	BAC03C	BMB03-	DIAD03	DABT03	EAC03	SCAN3	--
L							
M	BAC04C	BMB03+	DIAD04	DABT04	EAC04	DEVSL1	--
N							
P	BAC05C	BMB04-	DIAD05	DABT05	EAC05	DEVSL2	--
R							
S	BAC06C	BMB04+	DIAD06	DABT06	EAC06	--	CK201A
T	BAC07C	BMB05-	DIAD07	DABT07	EAC07	--	CK201B
U							
V	BAC08C	BMB05+	DIAD08	DABT08	EAC08	--	CKTLPA

'B'

D	BAC09C	BMB06-	DIAD09	DABT09	EAC09	BKRQ1	PRYREQ	
E	BAC10C	BMB06+	DIAD10	DABT10	EAC10	BKAC1	SPSVC	
F								
H	BAC11C	BMB07-	DIAD11	DABT11	EAC11	BKRQ2	PGENB	
J								
K	IOP1C	BMB07+	--	--	--	BKAC2	BLKSEL	
L								
M	IOP2C	BMB08-	DICTL	--	--	BKRQ3	BLKBT0	
N								
P	IOP4C	BMB08+	5BREAK	--	--	BKAC3	BLKBT1	
R								
S	BT1C	BMB09+	ADDACC	--	--	BKRQ4	BLKBT2	
T	BT2AC	BMB10+	--	--	--	BKAC4	DTALST	
U								
V	BPCLRC	BMB11+	--	--	--	--	HERE*	

Diagram II-13. CABLE LAYOUT

TABLE II-1

BUFFERED ACCUMULATOR OUTPUTS

201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A01D, A02D	BAC00C	→	→	CAC00-	A01D
A01E, A02E	BAC01C	→	→	CAC01-	A01E
A01H, A02H	BAC02C	→	→	CAC02-	A01H
A01K, A02K	BAC03C	→	→	CAC03-	A01K
A01M, A02M	BAC04C	→	→	CAC04-	A01M
A01P, A02P	BAC05C	→	→	CAC05-	A01P
A01S, A02S	BAC06C	→	→	CAC06-	A01S
A01T, A02T	BAC07C	→	→	CAC07-	A01T
A01V, A02V	BAC08C	→	→	CAC08-	A01V
B01D, B02D	BAC09C	→	→	CAC09-	B01D
B01E, B02E	BAC10C	→	→	CAC10-	B01E
B01H, B02H	BAC11C	→	→	CAC11-	B01H

TABLE II-2

BUFFERED MEMORY BUFFER OUTPUT LINES

201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A03D, A04D	BMB00+			CMB00-	A02D
A03E, A04E	BMB01+			CMB01-	A02E
A03H, A04H	BMB02+			CMB02-	A02H
A03K, A04K	BMB03-				
A03M, A04M	BMB03+			CMB03-	A02M
A03P, A04P	BMB04-				
A03S, A04S	BMB04+			CMB04-	A02S
A03T, A04T	BMB05-				
A03V, A04V	BMB05+			CMB05-	A02V
B03D, B04D	BMB06-				
B03E, B04E	BMB06+			CMB06-	B02E
B03H, B04H	BMB07-				
B03K, B04K	BMB07+			CMB07-	B02K
B03M, B04M	BMB08-				
B03P, B04P	BMB08+			CMB08-	B02P
B03S, B04S	BMB09+			CMB09-	B02S
B03T, B04T	BMB10+			CMB10-	B02T
B03V, B04V	BMB11+			CMB11-	B02V

TABLE II-3

PROGRAMMED INPUT/OUTPUT CONTROL

201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B01K, B02K	IOP1C	→	→	CIOP1	B01K
B01M, B02M	IOP2C	→	→	CIOP2	B01M
B01P, B02P	IOP4C	→	→	CIOP4	B01P

TABLE II-4

DATA-BREAK ADDRESS LINES

201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A05D, A06D	DIAD00	*		DADD00	A03D
A05E, A06E	DIAD01	*		DADD01	A03E
A05H, A06H	DIAD02	*		DADD02	A03H
A05K, A06K	DIAD03	*		DADD03	A03K
A05M, A06M	DIAD04	*		DADD04	A03M
A05P, A06P	DIAD05	*		DADD05	A03P
A05S, A06S	DIAD06	*		DADD06	A03S
A05T, A06T	DIAD07	*		DADD07	A03T
A05V, A06V	DIAD08	*		DADD08	A03V
B05D, B06D	DIAD09	*		DADD09	B03D
B05E, B06E	DIAD10	*		DADD10	B03E
B05H, B06H	DIAD11	*		DADD11	B03H

*Note: Collector of a Grounded-Emitter Transistor.

TABLE II-5

DATA-BREAK INPUT LINES

201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A07D, A08D	DABT00	*		DBIT00	A04D
A07E, A08E	DABT01	*		DBIT01	A04E
A07H, A08H	DABT02	*		DBIT02	A04H
A07K, A08K	DABT03	*		DBIT03	A04K
A07M, A08M	DABT04	*		DBIT04	A04M
A07P, A08P	DABT05	*		DBIT05	A04P
A07S, A08S	DABT06	*		DBIT06	A04S
A07T, A08T	DABT07	*		DBIT07	A04T
A07V, A08V	DABT08	*		DBIT08	A04V
B07D, B08D	DABT09	*		DBIT09	B04D
B07E, B08E	DABT10	*		DBIT10	B04E
B07H, B08H	DABT11	*		DBIT11	B04H

*Note: Collector of a Grounded-Emitter Transistor.

TABLE II-6

DATA BREAK CONTROL SIGNALS

201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B05M, B06M	DICTL	—◇ *	—◇	TRADI	B03M
B05P, B06P	BBREAK	→	→	CBBRK	B03P
B05S, B06S	ADDACC	→	→	CADACP	B03S
B01S, B02S	BTIC	→	→	CBT1	B01S
B01T, B02T	BT2AC	→	→	CBT2A	B01T
B01V, B02V	BPCLRC	→	→	CPWCLR	B01V

*Note: Collector of a Grounded-Emitter Transistor.

TABLE II-7

DATA BREAK REQUEST AND SELECT

201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B11D	BKRQ1			REQ2	D01D
B11E	BKAC1			SEL2	D01E
B11H	BKRQ2			REQ3	D01H
B11K	BKAC2			SEL3	D01K
B11M	BKRQ3			REQ4	D01M
B11P	BKAC3			SEL4	D01P
B11S	BKRQ4			REQ5	D01S
B11T	BKAC4			SEL5	D01T

TABLE II-8

EXTENDED ACCUMULATOR INPUTS

201A LINE ADAPTOR			SCANNER		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A09D, A10D	EAC00	*		EAC00+	A07D, A08D
A09E, A10E	EAC01	*		EAC01+	A07E, A08E
A09H, A10H	EAC02	*		EAC02+	A07H, A08H
A09K, A10K	EAC03	*		EAC03+	A07L, A08K
A09M, A10M	EAC04	*		EAC04+	A07M, A08M
A09P, A10P	EAC05	*		EAC05+	A07P, A08P
A09S, A10S	EAC06	*		EAC06+	A07S, A08S
A09T, A10T	EAC07	*		EAC07+	A07T, A08T
A09V, A10V	EAC08	*		EAC08+	A07V, A08V
B09D, B10D	EAC09	*		EAC09+	B07D, B08D
B09E, B10E	EAC10	*		EAC10+	B07E, B08E
B09H, B10H	EAC11	*		EAC11+	B07H, B08H

*Note: Collector of a Grounded-Emitter Transistor.

TABLE II-9

SCAN ADDRESS

201A LINE ADAPTOR			SCANNER		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A11D, A12D	SCAN 0	⟶	⟶	BXMT-	C03D
A11E, A12E	SCAN 1	⟶	⟶	BAD1-	C03E
A11H, A12H	SCAN 2	⟶	⟶	BAD2-	C03H
A11K, A12K	SCAN 3	⟶	⟶	BAD3-	C03K
B12M	BLKBT0	⟶	⟶	GND	D01M
B12P	BLKBT 1	⟶	⟶	GND	D01P
B12S	BLKBT2	⟶	⟶	GND	D01S

TABLE II-10

SCANNER CONTROL SIGNALS

201A LINE ADAPTOR			SCANNER		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B12D	PRYREQ	*	*	PORQ+	D01D
B12E	SPSVC	*	*	SSO+	D01E
B12H	PGENB	*	*	PGENB+	D01H
B12K	BLKSEL			BKSLO-	D01K
B12T	DTALST	*	*	DLOST+	D01T
B12V	HERE*	*	*	LACHK-	D01V
A11M, A12M	DEVSL1			DSL+	C03M
A11P, A12P	DEVSL2			ESL+	C03P

*Note: Collector of a Grounded-Emitter Transistor

TABLE II-11

TRANSMIT CLOCK

201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A13S, A14S	CK201A	→	→	CK2000	D03S
A13T, A14T	CK201B	→	→	CK240C	D03T
A13V, A14V	CKTLPA	→	→		

PANEL 1 ... COMM SECTION

	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16
	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	R107	R107
A																
B																
C																
D	BAC00C	BAC00C	BMB00+	BMB00+	DIAC00	DIAC00	DABTC0	CABTC0	EAC00	EAC00	SCAN0	SCAN0	JPA13D	JPA13C	BAC00	BMB00
E	BAC01C	BAC01C	BMB01+	BMB01+	DIAC01	DIAC01	DABTC1	CABTC1	EAC01	EAC01	SCAN1	SCAN1	JMA13E	JMA13E	BAC00C	BMB00+
F															BAC01	BMB01
H	BAC02C	BAC02C	BMB02+	BMB02+	DIAC02	DIAC02	DABTC2	CABTC2	EAC02	EAC02	SCAN2	SCAN2	JPA13H	. 13H	BAC01C	BMB01+
J															BAC02	BMB02
K	BAC03C	BAC03C	BMB03-	BMB03-	DIAC03	DIAC03	DABTC	CABTC3	EAC03	EAC03	SCAN3	SCAN3	JPA13K	JMA13K	BAC02C	BMB02+
L																BMB03
M	BAC04C	BAC04C	BMB03+	BMB03+	DIAC04	DIAC04	CABTC4	CABTC4	EAC04	EAC04	DEVSL1	DEVSL1	JPA13M	JMA13M		BMB03+
N															BAC04	BMB04
P	BAC05C	BAC05C	BMB04-	BMB04-	DIAC05	DIAC05	CABTC5	CABTC5	EAC05	EAC05	DEVSL2	DEVSL2	JPA13P	JMA13P	BAC04C	BMB04+
R																BMB05
S	BAC06C	BAC06C	BMB04+	BMB04+	DIAC06	DIAC06	CABTC6	CABTC6	FAC06	FAC06	JPA11S	JPA11S	CK201A	CK201A		BPB05+
T	BAC07C	BAC07C	BMB05-	BMB05-	DIAC07	DIAC07	DABTC7	CABTC7	EAC07	EAC07	JMA11T	JMA11T	CK201B	CK201B	BKSL3	BKSL1
U															BKAC3	BKAC1
V	BAC08C	BAC08C	BMB05+	BMB05+	DIAC08	DIAC08	DABTC8	CABTC8	EAC08	EAC08	JMA11V	JMA11V	CKTLPA	CKTLPA		

	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16
	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	W554	R111	R107	R107
A																
B																
C																
D	BAC09C	BAC09C	BMB06-	BMB06-	DIAC09	DIAC09	DABTC9	CABTC9	EAC09	EAC09	BKRQ1	PRYREQ	CK201A	SCNSVC	BAC06	BMB06
E	BAC10C	BAC10C	BMB06+	BMB06+	DIAC10	DIAC10	DABT10	CABT10	EAC10	EAC10	BKAC1	SPSVC	CK201A		BAC06C	BMB06+
F													CK201A		BAC07	BMB07
H	BAC11C	BAC11C	BMB07-	BMB07-	DIAC11	DIAC11	DABT11	CABT11	EAC11	EAC11	BKRQ2	PGENB	CK201A	SCSVCA	BAC07C	BMB07+
J													CK201B	SCSVCB	BAC08	BMB08
K	1UP1C	1UP1C	BMB07+	BMB07+	JPB05K	JMB05K	CYSEL	CYSEL	RDENB	RDENB	BKAC2	BLKSEL	CK201B	SCSVCB	BAC08C	BMB08+
L													CK201B		BAC09	BMB09
M	1UP2C	1UP2C	BMB08-	BMB08-	CICTL	CICTL	JPB07M	JPB07M	SKENB	SKENB	BKRC3	BLKBTO	CK201B		BAC09C	BMB09+
N														PRYREQ	BAC10	BMB10
P	1UP4C	1UP4C	BMB08+	BMB08+	EBREAK	BRREAK	JPB07P	JPB07P	JPB09P	JPB09P	BKAC3	BLKBT1		SCNSVC	BAC10C	BPB10+
R														SCSVCB	BAC11	BMB11
S	BT1C	BT1C	BMB09+	BMB09+	ACLACC	ADCACC	JPB07S	JPB07S	JMB09S	JPB09S	BKRC4	ELKBT2	1SCTE		BAC11C	BMB11+
T	PT2AC	PT2AC	BMB10+	BMB10+	JMB05T	JMB05T	JMB07T	JMB07T	JMB09T	JMB09T	BKAC4	DTALST	2SCTE		BACTY	BKSL2
U													3SCTE	SPSVC	BAC09C	BKAC2
V	BPCLRC	BPCLRC	BMB11+	BMB11+	JMB05V	JMB05V	JMB07V	JPB07V	JMB09V	JMB09V		HERE*	4SCTE			

TABLE II-12.

PANEL 1 ... COMMON SECTION

	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32
	R1C7	R111					WOSC	WCSC								
A																
B																
C																
D	SCANC-	BLKBTC														
E	SCANC	BLKAC					1SRSV+	2SRSV+								
F	SCANC+															
H	SCANC-	DIADC7					1DLST+	2DLST+								
J	SCAN1-															
K	SCAN1	BLKBT1					1PAR+	2PAR+								
L	SCAN1+	BLKAC														
M	SCAN1-						1STRDY	2STRDY								
N	SCAN2-	DIACC6														
P	SCAN2						1TMRD+	2TMRC+								
R	SCAN2+	BLKBT2														
S	SCAN2-	BLKAC					1XMT+	2XMT+								
T	BKSL4															
U	BKAC4	DIACC5					1REC+	2REC+								
V																

	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32
	R1C7	R111	ROC1				WCSC	WOSC								
A																
B																
C																
D	SCAN3-	BKAC1	BKAC3													
E	SCAN3	BKAC2	BLKND				3SRSV+	4SRSV+								
F	SCAN3+	BLKNC	BKAC4													
H	SCAN3-	BLKAC	BLKNC				3DLST+	4DLST+								
J	BKSLD	BLKAC														
K	BLKSEL	BLKAC					3PAR+	4PAR+								
L	BPCLR															
M	BPCLRC						3STRDY	4STRDY								
N	CTWD1	PCENB														
P	DEVSL1						3TMRD+	4TMRC+								
R	CTWD2	BT1C														
S	DEVSL2						3XMT+	4XMT+								
T	IOP4															
U	IOP4C	BT1					3REC+	4REC+								
V		BT1														

TABLE II-13.

PANEL 2 ... PORT O/LINE ADAPTOR 1

	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16	
	W2C1C	E1AR	R111	W501	R111	R001	R302	R111	R201	R205	R205	R205	R2C5	R205	R201	R205	
A																	A
B																	B
C		1GNDC2		1GND04			1GNC06									1GND14	C
D	1SCB	1GND02	1RD+	1SRCK	1SCHF+	1REC-		1RECE-		1SHIFT	1SHIFT	1SHIFT	1SHIFT	1SHIFT		1SHIFT	D
E	1RCB	1RINGP	1REC+		1LINE+	1OTND1	1ROSC+		1SHIFT	1SR01-	1SR03-	1SR05-	1SR07-	1SR09-	1SHIFT	1SDBF+	E
F	1RSB			1SRCK	1LTAC1	1REC-	1GND06		1RD+	1ZERSR	1ZERSR	1ZERSR	1ZERSR	1ZERSR	1SR10+		F
H	1CSCB	1RING	1RD-		1CLT1	1OTND2		1REC+		BMB01	BMB03	BMB05	BMB07	BMB09		1GND14	H
J	1SROB	1RING	1RD-		1OLT1	1REC-	1A06JK			1SR01+	1SR03+	1SR05+	1SR07+	1SR09+			J
K	1TRDYB	1GNDC2	1DLS1+		1PTBF+	1RSND	1A06JK	1XMTE-	1ZRCSR	1SR00-	1SR02-	1SR04-	1SR06-	1SR08-	1ZERSR	1SR11+	K
L	1RINGB	1CSDB		1GND04	1LINE-				1SR00+	1SR0C+	1SR02+	1SR04+	1SR06+	1SR08+	1SR11+	1SR11-	L
M	1CCETB	1DELAY		1L04	1CTAD2		1BFIX		1SR00-	1MBSR	1MBSR	1MBSR	1MBSR	1MBSR	1SR11-	1FRZE	M
N		1CS+	DTALST	1L04	1CLT1		1IFMD<	1XMT+		1SHIFT	1SHIFT	1SHIFT	1SHIFT	1SHIFT		1SHIFT	N
P	1SCTB	1CS+					1REC-		1SHIFT	1SR02+	1SR04+	1SR06+	1SR08+	1SR10+	1SHIFT	1PATY+	P
R	1SCRB	1GNDC2	1BFIX	1SCRB	1XMT-				1RD-	1SR02-	1SR04-	1SR06-	1SR08-	1SR10-	1SR10-	1PATY-	R
S		1SRDB			1XTRG+		1A06ST		1MBSR	BMB02	BMB04	BMB06	BMB08	BMB10	1MBSR	1GND14	S
T					1RSND		1A06ST		BMB00	1SR01-	1SR03-	1SR05-	1SR07-	1SR09-	BMB11	1EP2	T
U		1STRDY	1DELAY		1RS1					1SR01+	1SR03+	1SR05+	1SR07+	1SR09+		1EP2	U
V	1HERE	1STRDY			1RS1		1BR1			1MBSR	1MBSR	1MBSR	1MBSR	1MBSR		1ZROSR	V

	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16	
	W6C2	E1AR	W6C2	W501	W501	R202	R602	R6C2	R602	R602	R202	R107	R1C7	R121	R111	R002	
A																	A
B																	B
C		1GND34		1GND35							1GND43						C
D	1CUT1	1GND34	1SCTE	1SCK	1CCTD		1JMP39	1JMP40	1JMP41		1SRSV+	1CARDT	1BRENB	1IOPCS	1ENDI	1SR00-	D
E		1RDB			1CCT			1FR3+			1RSYN-	1CDTD	1BR1	1EBPC+	1BRENB	1SR01-	E
F	1SCB		1SCTE	1SCK	1CCTD	1PWCLR		1EXMT			1PWCLR	1DY+	BKRQ1	1DTSY+		1DSYND	F
H	1RCSL+	1RCP1				1REC-	1CLOCK	1BRKON		1CLOCK	1RSYN-	1DY-	1BKRC+	1F1	1CHRON	1SR02-	H
J		1RDBI				1REC+	1DTSY-	1ENZR		1SYNC-	1RSYN+	1STCK	1ENAX+	1IFMD-	1CHRON	1SR03+	J
K	1RSB	1GND34			1L37	1SRCK	1ZERSR	1ZROSR	1PWCLR	1START	1SRSV-	1SCK	1ENAX-	1DTSY-	1IFMD-	1DSYND	K
L	1TMRC+	1CDETB		1GND36	1L37	1RFCB-	1ZROSR	1START	BPCLR		1REC-	1RD+	1ENBL+	1ESFT	1REC+	1SR04-	L
M				1L36	1L37		1JMP39	1JMP40	1JMP41			1RDP	1ENBL-	1DY-	1DSYND	1SR05+	M
N	1TRDYB	1CUT		1L36	1L37						1START	1DTSY+	1ENDI	1SVC-	1DTSY-	1DSYND	N
P	1V+BC1	1CCT	1V+BC3				1STCK				1GND43	1DTSY-	1END	1IOPCS	1DTSY-	1SR06+	P
R	1V-BC1		1V-BC3	1SCTB	1JMP37	1PWCLR	1XMT-				1PWCLR	1CS-	1HEREB	1EFR0		1SR07-	R
S	1V+BC1		1V+BC3		1CCT	1XMT-	1SRCK	1CLOCK	1BRKON		1SYNC-	1CS+	1HERE	1F1		1DSYND	S
T					1JMP37	1XMT+	1REC-	1ESFT	1EXMT				1BLOCK	1SVC-		1HEREB	T
U						1STCK	1CLOCK	1SHIFT	1MBSR	1END	1CLOCK		BKSLB	1IOPCS		1BLOCK	U
V	1V-BC1		1V-BC3			1XMTE-				1FR3+	1SVC-				1END1	1HERND	V

TABLE II-14.

PANEL 2 ... PORT O/LINE ADAPTOR 1

	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32	
	R202	R123	R123	R201	R201	R201	R205	R205	R205	R205	R123	R123	W994	R123	R111		
A																	A
B																	B
C					1GND19	1GND20											C
D	1FR3+	1SR00+	1SR06+				1INVMK	1INVMK	1STCK	1BRKON	1SRSV+	1EBPC+	SCAN1+	1CFR3+	1ADR08		D
E	1DY-	1SR01+	1SR07+	1INVMK	1ADAC	1START			1CLSD-	1RQSD-	1DLST+	1IFMD+	SCAN1-	1CFR2+	BKSL1		E
F		BKSL1	BKSL1	BAC07	1GND19	1GND20	1PWCLR	1PWCLR	1PWCLR	1PWCLR	1ENBL+	1ENBL+	SCAN2+	1ENAX+			F
H	1LINE-	DABT00	DABT06	1REC-				1PAR1		1RS1	EAC00	EAC06	SCAN2-	EAC08	DIAD08		H
J	1LINE+	DABT01	DABT07	1XMT+			1EBPC+	1PAR+	1CLSD+	1RQSD+	EAC01	EAC07	SCAN3+	EAC09			J
K	1CLOCK	1SR02+	1SR08+	1PWCLR	1PWCLR	1PWCLR	BAC06	BAC02	1CS-	1XTRQ-	1PAR+	1STRDY	SCAN3-	1CFR1+	1ADR09		K
L	1LINE+	1SR03+	1SR09+	1IFMD+	1BKRQ+		BAC06	BAC02	1CS+	1XTRQ+	1RQSD+	1TMRD+	1SCAN1	1CFRQ+	BKSL1		L
M	1FRZE	BKSL1	BKSL1	1IFMD-		1SVC-		1CLOCK		BT1	1ENBL+	1ENBL+	1SCAN2	1ENAX+			M
N	1FR3+	DABT02	DABT08			1RSTRT	1INVMK	1INVMK	1INVMK	1INVMK	EAC02	EAC08	1SCAN3	EAC10	DIAD09		N
P	1PATY-	DABT03	DABT09	1INVMK	1FR1+	1REC-	1TMRD+	1DLST+	1SRSV+	1XTRQ+	EAC03	EAC09	1ADR08	EAC11			P
R		1SR04+	1SR10+	BAC07	1IFMD-	1XMT+			1SRSV-	1XTRQ-	1XTRQ+	1RING	1ADR09	1RQSD+	1ADR10		R
S	1PTBF+	1SR05+	1SR11+	1CLOCK	1START	1XMT-		1SRSV-	1ESRSV		1CLSD+	1CARDT	1ADR10	1RQSD+	BKSL1		S
T		BKSL1	BKSL1	1DTSY-	1XMT-	1REC+	BACTY	BAC01	BAC00	BAC04	1ENBL+	1ENBL+		BKSL1			T
U	1FR3+	DABT04	DABT10	1XMT-			BACTY	BAC01	BAC00	BAC04	EAC04	EAC10		DIAD11	DIAD10		U
V	1PATY+	DABT05	DABT11	1REC+				1CHRON	1CHRON		EAC05	EAC11		DICTL			V

	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32	
	R111	R002	R001	R111	R121	R121	R121	R001	R111	R603	R602	R205	R205	R205	R205		
A																	A
B																	B
C											1GND59	1GND60	1GND61				C
D	1SRSV+	1BLOCK	1TMRD+	1RQSD+		1EP2		CTW01	1SCAN1	1OP4	1JMP59	1CLOCK	1FR1+	1LDAUX	1LDAUX		D
E	1RSYN+	SCAN0-	1XMIND	1CLSD+		1RD+		1BLND	1SCAN2	1ENB1				1CFR0-	1CFR2-		E
F	1SNIND	1SNIND	1CARDT	1XMIND		1DTSY+		1BLOCK	1BLND	1INVMK		1FRZE	1FRZE	1PWCLR	1PWCLR		F
H	SCNSVC	1SCAN1	1XMIND	1XMTE-	1FNZR	1EP2	1ADAC	1BLND	1ENBL-		1SVC-	1CFR0-	1CFR2-				H
J		1SCAN2	1STRDY	1XMTE-	1REC+	1SR11+	ADDACC	CTW02	1ENBL-		1GND59	1FR0+	1FR2+	1CFR0+	1CFR2+		J
K	1SRSV+	1SNIND	1XPTND	1FR3+	1IFMD+	1XMT+	BKSL1	1AXND	1SCAN1	1ZRUSH	1FRZE	1EFRO	1GND61	BAC11	BAC09		K
L	1XMT+	1BLOCK	1FR2+	1FR0+	1EXMT	1EP2	1BRKON	1BLOCK	1SCAN2	1XTRQ+	1PWCLR	1EFRO	1GND61	BAC11	BAC09		L
M	1SN2ND	SCAN0+	1DYNC	1CYND	1IFMD+	1RD+	BKSL1	1AXND	1AXND	1LDFR	1JMP59	1LDFR	1LDFR				M
N	SCNSVC	1SN2ND	1FR1+	1CY-	1XTRQ+	1REC+	BBREAK	1REC+	1ENAX-			1FRD+	1FR2+	1LDAUX	1LDAUX		N
P		1SCAN1	1DYNC	1CY-	1XMT+	1IFMD+	BT1C	1PARND	1ENAX-	1MBSK	1IFMD-	1FR1+	1FR3+	1CFR1+	1CFR3+		P
R		1SCAN2	1EBPC+	1REC+	1RECE-	1ESRSV	1PAR1	1CY+	1RD+	1OP4	1XMT-			1CFR1-	1CFR3-		R
S	1SCAN3	1SN2ND	1DYNC	1IFMD+	1FCSC-	1XMT+	1RD-	1PARND	1PATY-	1ENAX-	1IFMD+	1CFR1-	1CFR3-				S
T	1HERND	1SCAN1	1IFMD+		1CLSE-	1XTRQ+	1REC+		1PARND	1LDAUX	1REC-	1GND60	1GND61	BAC10	BAC08		T
U	HERE+	1SCAN2	1DYNC	1ESRSV	[illegible]	1IFMD+	1CY+		1PAR1		1RSTRT	1GND60	1GND61	BAC10	BAC08		U
V		1FERND			1STRDY		1PATY+					1LDFR	1LDFR				V

TABLE II-15.

PANEL 3 ... PORT 1/LINE ADAPTER 2

	AC1	AC2	AC3	A04	AC5	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16	
	W2?1C	EIAR	R111	W502	R111	R001	R302	R111	R201	R205	R205	R205	R205	R205	R201	R205	
A																	A
B																	B
C		2GND02		2GND04			2GND06									2GND14	C
D	2SCB	2GND02	2RD+	2SRCK	2SEBF+	2REC-		2RECE-		2SHIFT	2SHIFT	2SHIFT	2SHIFT	2SHIFT		2SHIFT	D
E	2RCB	2RINGB	2REC+		2LINE+	2DTN01	2RQSO+		2SHIFT	2SR01-	2SR03-	2SR05-	2SR07-	2SR09-	2SHIFT	2SDBF+	E
F	2RSB			2SRCK	2CTNC1	2REC-	2GND06		2RO+	2ZERSR	2ZERSR	2ZERSR	2ZERSR	2ZERSR	2SR10+		F
H	2CSDB	2RING	2RD-		2CLTI	2DTN02		2REC+		BMB01	BMB03	BMB05	BMB07	BMB09		2GND14	H
J	2SRCB	2RING	2RD-		2CLTI	2REC-	2A06JK			2SR01+	2SR03+	2SR05+	2SR07+	2SR09+			J
K	2TRDYB	2GND02	2DLSI+		2FTBF+	2RSND	2A06JK	2XMTE-	2ZRDSR	2SR00-	2SR02-	2SR04-	2SR06-	2SR08-	2ZERSR	2SR11+	K
L	2RINGE	2CSDB		2GND04	2LINE-				2SR00+	2SR00+	2SR02+	2SR04+	2SR06+	2SR08+	2SR11+	2SR11-	L
M	2CCETE	2DELAY		2L04	2CINC2		2BFIX		2SRC0-	2MBSR	2MBSR	2MBSR	2MBSR	2MBSR	2SR11-	2FRZE	M
N		2CS+	DTALST	2L04	2CLT:		2IFMO+	2XMT+		2SHIFT	2SHIFT	2SHIFT	2SHIFT	2SHIFT		2SHIFT	N
P	2SCTB	2CS+					2REC-		2SHIFT	2SR02+	2SR04+	2SR06+	2SR08+	2SR10+	2SHIFT	2PATY+	P
R	2SCRB	2GND02	2BFIX	2SCRB	2XP1-				2RD-	2SR02-	2SR04-	2SR06-	2SR08-	2SR10-	2SR10-	2PATY-	R
S		2SRDB			2XTFC+		2A06ST		2MBSR	BMB02	BMB04	BMB06	BMB08	BMB10	2MBSR	2GND14	S
T					2RSNC		2A06ST		BMB00	2SR01-	2SR03-	2SR05-	2SR07-	2SR09-	BMB11	2EP2	T
U		2STRDY	2DELAY		2RS1					2SR01+	2SR03+	2SR05+	2SR07+	2SR09+		2EP2	U
V	2HERE	2STRDY			2RS1		2BR1			2MBSR	2MBSR	2MBSR	2MBSR	2MBSR		2ZROSR	V

	BC1	BC2	BC3	B04	BC5	B06	B07	B08	BC9	B10	B11	B12	B13	B14	B15	B16	
	W602	EIAR	W602	W501	W501	R202	R602	R602	R602	R602	R202	R107	R107	R121	R111	R002	
A																	A
B																	B
C		2GND34		2GND36							2GND43						C
D	2CLTI	2GND34	2SCTE	2SCK	2CCTC		2JMP39	2JMP40	2JMP41		2SRSV+	2CARDT	2BRENB	2IGPCS	2ENOI	2SR00-	D
E		2RDB			2CDT			2FR3+			2RSYN-	2COTO	2BRI	2EBPC+	2BRENB	2SR01-	E
F	2SCB		2SCTB	2SCK	2CCTL	2PWCLR		2EXMT			2PWCLR	2DY+	BKRC2	2DTSY+		2DSYND	F
H	2PGSD+	2RCBI				2REC-	2CLOCK	2BRKDN		2CLOCK	2RSYN-	2DY-	2BKRC+	2F1	2CHRDN	2SR02-	H
J		2RDBI				2REC+	2DTSY-	2ENZR		2SYNC-	2RSYN+	2STCK	2ENAX+	2IFMO-	2CHRDN	2SR03+	J
K	2RSB	2GND34			2D37	2SRCK	2ZERSR	2ZRDSR	2PWCLR	2START	2SRSV-	2SCK	2ENAX-	2DTSY	2IFMO-	2DSYND	K
L	2IMRC+	2CDETB		2GND36	2D37	2RECE-	2ZRCSR	2START	BPCLR		2REC-	2RD+	2ENBL+	2ESFT	2REC+	2SR04-	L
M				2L36	2L37		2JMP39	2JMP40	2JMP41			2RDBI	2ENBL-	2DY-	2DSYNO	2SR05+	M
N	2TRDYP	2CDT		2L36	2L37						2START	2DTSY+	2ENDI	2SVC-	2DTSY-	2DSYND	N
P	2V+BC1	2CDT	2V+B03				2STCK				2GND43	2DTSY-	2ENO	2IDPCS	2DTSY-	2SR06+	P
R	2V-BC1		2V-B03	2SCTB	2JM37	2PWCLR	2XM1-				2PWCLR	2CS-	2HEREB	2EFRO		2SR07-	R
S	2V+BC1		2V+B03		2CCT	2XMT-	2SRCK	2CLOCK	2RRKDN		2SYNC-	2CS+	2HERE	2F1		2DSYND	S
T					2JP37	2XMT+	2REC-	2ESFT	2EXMT				2BLOCK	2SVC-		2HEREB	T
U						2STCK	2CLOCK	2SHIFT	2MBSR	2ENO	2CLOCK		BKSLB	2IOPCS		2BLCCK	U
V	2V-BC1		2V-B03			2XMTE-				2FR3+	2SVC-				2ENDI	2HERND	V

PANEL 3 ... PORT 1/LINE ADAPTER 2

	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32
	R 22	R123	R123	R201	R201	R201	R205	R205	R205	R205	P123	R123	W554	R123	R111	
A																
B																
C					2GND19	2GND20										
D	2FR3+	2SRC0+	2SR06+				2INVMK	2INVMK	2STCK	2BRKDN	2SRSV+	2EBPC+	SCAN1+	2CFR3+	2ADR08	
E	2DY-	2SRC1+	2SRC7+	2INVMK	2ADAC	2START			2CLSD-	2RDSC-	2DLST+	2IFMD+	SCAN1-	2CFR2+	BKSL2	
F		BKSL2	BKSL2	BAC07	2GND19	2GND20	2PWCLR	2PWCLR	2PWCLR	2PWCLR	2ENBL+	2ENBL+	SCAN2+	2ENAX+		
H	2LINE-	DABT00	DABT06	2REC-				2PAR1		2RS1	EAC00	EAC06	SCAN2-	EAC08	D1AD08	
J	2LINE+	DABT01	DABT07	2XMT+			2FBFC+	2FAR+	2CLSC+	2RQSD+	EAC01	EAC07	SCAN3+	EAC09		
K	2CLOCK	2SRC2+	2SRC8+	2PWCLR	2PWCLR	2PWCLR	BAC06	EAC02	2CS-	2XTRQ-	2PAR+	2STRDY	SCAN3-	2CFR1+	2ADR09	
L	2LINE+	2SRC3+	2SRC9+	2IFMD+	2BKRQ+		BAC06	BAC02	2CS+	2XTRQ+	2RQSD+	2TMRD+	2SCAN1	2CFR0+	BKSL2	
M	2FRZE	BKSL2	BKSL2	2IFMD-		2SVC-		2CLOCK		RT1	2ENBL+	2ENBL+	2SCAN2	2ENAX+		
N	2FR3+	DABT02	DABT08			2RSTRT	2INVMK	2INVMK	2INVMK	2INVMK	EAC02	EAC08	2SCAN3	EAC10	D1AD09	
P	2PATY-	DABT03	DABT09	2INVMK	2FR3+	2REC-	2TMRC+	2CLST+	2SRSV+	2XTRQ+	EAC03	EAC09	2ADRC8	EAC11		
R		2SR04+	2SR10+	BAC07	2IFMD-	2XMT+			2SRSV-	2XTRC-	2XTRQ+	2RING	2ADRC9	2RQSD+	2ADR10	
S	2PTBF+	2SRC5+	2SR11+	2CLOCK	2START	2XMT-		2SRSV-	2ESRSV		2CLSD+	2CARDT	2ADR10	2RCSD+	BKSL2	
T		BKSL2	BKSL2	2DTSY-	2XMT-	2REC+	BACTY	BAC01	BAC00	EAC04	2ENBL+	2ENBL+		BKSL2		
U	2FR3+	DABT04	DABT10	2XMT-			BACTY	BAC01	BAC00	BAC04	EAC04	EAC10		C1AC11	C1AD10	
V	2PATY+	DABT05	DABT11	2REC+				2CHRCN	2CHRDN		EAC05	EAC11		DICTL		

	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32
	R111	R002	R001	R111	R121	R121	R121	R001	R111	R603	R602	R205	R205	R205	R205	
A																
B																
C											2GND59	2GND60	2GND61			
D	2SRSV+	2BLLCK	2TMRD+	2RQSD+		2EP2		CTWD1	2SCAN1	10P4	2JMP59	2CLOCK	2FR1+	2LDAUX	2LDAUX	
E	2RSYN+	SCAN0-	2XMIND	2CLSD+		2RD+		2BLNC	2SCAN2	2ENBL-				2CFR0-	2CFR2-	
F	2SNIND	2SNIND	2CARDT	2XMIND		2DTSY+		2BLLCK	2BLNC	2INVMK		2FRZE	2FRZE	2PWCLR	2PWCLR	
H	SCNSVC	2SCAN1	2XMIND	2XMTF-	2EN/R	2EP2	2ADAC	2BLNC	2ENBL-		2SVC-	2CFR0-	2CFR2-			
J		2SCAN2	2STRDY	2XMTE-	2REC+	2SR11+	ADDACC	CTWD2	2ENBL-		2GND59	2FR0+	2FR2+	2CFR0+	2CFR2+	
K	2SRSV+	2SNIND	2XMIND	2FR3+	2IFMD+	2XMT+	BKSL2	2AXNC	2SCAN1	2ZRDSR	2FRZE	2EFRO	2GND61	BAC11	BAC09	
L	2XMT+	2BLLCK	2FP2+	2FRC+	2EXMT	2EP2	2BRKDN	2BLOCK	2SCAN2	2XTRQ+	2PWCLR	2EFRO	2GND61	BAC11	BAC09	
M	2SN2ND	SCANC+	2DYND	2DYND	2IFMD+	2RD+	BKSL2	24XNC	2AXND	2LDFR	2JMP59	2LDFR	2LDFR			
N	SCNSVC	2SN2ND	2FR1+	2DY-	2XTRQ+	2REC+	BBREAK	2RFC+	2ENAX-			2FR0+	2FR2+	2LDAUX	2LDAUX	
P		2SCAN1	2DYNC	2DY-	2XMT+	2IFMD+	BT1C	2PARND	2ENAX-	2MBSR	2IFMD-	2FR1+	2FR3+	2CFR1+	2CFR3+	
R		2SCAN2	2EBPC+	2REC+	2RECE-	2ESRSV	2PAR1	2DY+	2RD+	10P4	2XMT-			2CFR1-	2CFR3-	
S	2SCAN3	2SN2ND	2DYNC	2IFMD+	2FLSC-	2XMT+	2RD-	2PARND	2PATY-	2ENAX-	2IFMD+	2CFR1-	2CFR3-			
T	2HERND	2SCAN1	2IFMD+		2CLSC-	2XTRQ+	2REC+		2PARNC	2LDAUX	2REC-	2GND60	2GND61	BAC10	BAC08	
U	HERE+	2SCAN2	2DYND	2ESRSV	2CARDT	2IFMD+	2DY+		2PAR1		2RSTRT	2GND60	2GND61	BAC10	BAC08	
V		2HERND			2STRDY		2PATY+					2LDFR	2LDFR			

TABLE II-17.

PANEL 4 ... PORT 2/LINE ADAPTER 3

	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16
	W201C	L1AP	R111	W501	R111	R001	R302	R111	R201	R205	R205	R205	R205	R205	R2C1	R205
A																
B																
C		3GND02		3GND04			3GND06									3GND14
D	3SCh	3GND02	3RD+	3SRCK	3SCHF+	3REC-		3RECE-		3SHIFT	3SHIFT	3SHIFT	3SHIFT	3SHIFT		3SHIFT
E	3RCA	3RINGH	3REC		3LINE+	3CINDI	3POSL+		3SHIFT	3SR01-	3SR03-	3SR05-	3SR07-	3SR09-	3SHIFT	3SDBF+
F	3RS[illegible]			3SRCK	3CINDI	3REC-	3GND06		3RC+	3ZERSR	3ZERSR	3ZERSR	3ZERSR	3ZERSR	3SR10+	
H	3CSCE	3RING	3RC-		3CLT1	3DTND2		3RFC+		8MB01	8MB03	8MB05	8MB07	8MB09		3GND14
J	3SRCB	3RING	3RD-		3CLT1	3REC-	3AC6JK			3SR01+	3SR03+	3SR05+	3SR07+	3SR09+		
K	3TRDYE	3GND02	3DLST+		3PTBF+	3RSND	3AC6JK	3XMTF-	3ZRLSR	3SR00-	3SR02-	3SR04-	3SR06-	3SR08-	3ZERSR	3SR11+
L	3RINGE	3CNCE		3GND04	3LINE-				3SR10+	3SR00+	3SR02+	3SR04+	3SR06+	3SR08+	3SR11+	3SR11-
M	3CLETE	3DELAY		3L04	3CTND2		3EFIX		3SR09-	3MBSR	3MBSR	3MBSR	3MBSR	3MBSR	3SR11-	3FRZE
N		3CS+	DTALST	3L04	3CLT1		3IFMD+	3XMT+		3SHIFT	3SHIFT	3SHIFT	3SHIFT	3SHIFT		3SHIFT
P	3SCTE	3CS+					3REC-		3SHIFT	3SR02+	3SR04+	3SR06+	3SR08+	3SR10+	3SHIFT	3PATY+
R	3SCXE	3GND02	3EFIX	3SCR8	3XMT-				3RC-	3SR02-	3SR04-	3SR06-	3SR08-	3SR10-	3SR10-	3PATY-
S		3SRCB			3XTFC+		3AC6ST		3MBSR	8MB02	8MB04	8MB06	8MB08	8MB10	3MBSR	3GND14
T					3FSNC		3AC6ST		8MB00	3SR01-	3SR03-	3SR05-	3SR07-	3SR09-	8MB11	3EP2
U		3STRDY	3DELAY		3FSI					3SR01+	3SR03+	3SR05+	3SR07+	3SR09+		3EP2
V	3HERE	3STRDY			3FSI		3RKI			3MBSR	3MBSR	3MBSR	3MBSR	3MBSR		3ZROSR

	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16
	W602	L1AP	W602	W501	W501	R202	R602	R602	R602	R602	R202	R107	R107	R121	R111	R002
A																
B																
C		3GND34		3GND36							3GND43					
D	3OUT1	3GND34	3SCTF	3SCK	3CLID		3JMP39	3JMP40	3JMP41		3SRSV+	3CARDT	3BRENB	3IOPCS	3ENDI	3SR00-
E		3RDE			3CCT			3FR3+			3RSYN-	3CDTD	3BR1	3EBPC+	3BRENB	3SR01-
F	[illegible]		3SCTB	3SCK	3CLTL	3PWCLR		3FXMT			3PWCLR	3DY+	8KRC3	3DTSY+		3DSYND
H	3RCSC+	3RDEI				3REC-	3CLOCK	3HRKDN		3CLOCK	3RSYN-	3DY-	3BKRC+	3F1	3CHRDN	3SR02-
J		3RDEI				3REC+	3DTSY-	3ENZR		3SYNC-	3RSYN+	3STCK	3ENAX+	3IFMD-	3CHRDN	3SR03+
K	[illegible]	3GND34			3L27	3SRCK	3ZERSR	3ZROSR	3PWCLR	3START	3SRSV-	3SCK	3ENAX-	3DTSY-	3IFMD-	3DSYND
L	3TMCL+	3CLETE		3GND36	3L27	3RFCE-	3ZRLSR	3START	3PCLR		3REC-	3RD+	3ENBL+	3ESFT	3REC+	3SR04-
M				3L36	3L27		3JMP39	3JMP40	3JMP41			3RDB1	3ENBL-	3DY-	3DSYND	3SR05+
N	3TRDYE	3CCT		3L36	3L27						3START	3DTSY+	3ENDI	3SVC-	3DTSY-	3DSYND
P	3V+H01	3CCT	3V+H03				3STCK				3GND43	3DTSY-	3END	3IOPCS	3DTSY-	3SR06+
R	3V-H01		3V-H03	3SCTB	3JMP37	3PWCLR	3XMT-				3PWCLR	3CS-	3HEREB	3EFRO		3SR07-
S	3V+B01		3V+H03		3CLT	3XMT-	3SRCK	3CLOCK	3HRKDN		3SYNC-	3CS+	3HERE	3F1		3DSYND
T					3JMP37	3XMT+	3REC-	3CSFT	3EXMT				3BLOCK	3SVC-		3HEREB
U						3STCK	3CLOCK	3SHIFT	3MBSR	3END	3CLOCK		8KSLB	3IOPCS		3BLOCK
V	3V-H01		3V-H03			3XMTE-				3FR3+	3SVC-				3ENDI	3HERND

TABLE II-18.

PANEL 4 ... PORT 2/LINE ADAPTOR 3

	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32
	R202	R123	R123	R201	R201	R201	R205	R205	R205	R205	R123	R123	R554	R123	R111	
A																
B																
C					3GAC19	3GND20										
D	3FR3+	3SR00+	3SR06+				3INVMK	3INVMK	3STCK	3BRKDN	3SRSV+	3EBPC+	SCAN1+	3CFR3+	3ADR08	
E	3DY-	3SR01+	3SR07+	3INVMK	3ACAC	3START			3CLSD-	3RESC-	3CLST+	3IFMC+	SCAN1-	3CFR2+	BKSL3	
F		BKSL3	BKSL3	EAC07	3GAD19	3GND2C	3PWCLR	3PWCLR	3PWCLR	3PWCLR	3ENBL+	3ENBL+	SCAN2+	3ENAX+		
H	3LINE-	DABTC0	DABT06	3REC-				3PAR1		3RS1	EAC00	EAC06	SCAN2-	EAC08	DIAD08	
J	3LINE+	DABTC1	DABT07	3XMT+			3EBPC+	3PAR+	3CLSD+	3RQSD+	EAC01	EAC07	SCAN3+	EAC09		
K	3CLOCK	3SR02+	3SR08+	3PWCLR	3PWCLR	3PWCLR	BACC6	EACC2	3CS-	3XTRQ-	3PAR+	3STRDY	SCAN3-	3CFR1+	3ADR09	
L	3LINE+	3SR03+	3SR09+	3IFMO+	3BKRQ+		BAC06	BACC2	3CS+	3XTRQ+	3RQSD+	3TMRD+	3SCAN1	3CFR0+	BKSL3	
M	3FRZE	BKSL3	BKSL3	3IFMD-		3SVC-		3CLCCK		ET1	3ENBL+	3ENBL+	3SCAN2	3ENAX+		
N	3FR3+	DABTC2	DABT08			3RSTRT	3INVMK	3INVMK	3INVMK	3INVMK	EACC2	EAC08	3SCAN3	EAC10	DIAD09	
P	3PATY-	DABTC3	DABT09	3INVMK	3FR3+	3REC-	3TMRD+	3CLST+	3SRSV+	3XTRQ+	EAC03	EAC09	3ADR08	EAC11		
R		3SR04+	3SR10+	EAC07	3IFMD-	3XMT+			3SRSV-	3XTRQ-	3XTRQ+	3RING	3ADR09	3RQSD+	3ADR10	
S	3PTHF+	3SR05+	3SR11+	3CLCCK	3START	3XMT-		3SRSV-	3ESRSV		3CLSD+	3CARDT	3ADR10	3RQSD+	HKSL3	
T		BKSL3	BKSL3	3CTSY-	3XMT-	3REC+	BACTY	BACC1	BAC00	BAC04	3ENBL+	3ENBL+		BKSL3		
U	3FR3+	DABTC4	DABT10	3XMI-			BACTY	EACC1	BAC00	BACC4	EAC04	EAC10		DIAD11	DIAD10	
V	3PATY+	DABTC5	DABT11	3REC+				3CHRON	3CHRON		EAC05	EAC11		DICTL		

	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32
	R111	R002	R001	R111	R121	R121	R121	R001	R111	R603	R602	R205	R205	R205	R205	
A																
B																
C											3GND59	3GND60	3GAD61			
D	3SRSV+	3BLOCK	3TPRD+	3RQSD+		3EP2		CTWD1	3SCAN1	IOP4	3JMP59	3CLOCK	3FR1+	3LDAUX	3LDAUX	
E	3XSYN+	SCAN0-	3XMIND	3CLSD+		3RD+		3BLNC	3SCAN2	3ENBL-				3CFR0-	3CFR2-	
F	3SNIND	3SNIND	3CARDT	3XMIND		3DTSY+		3BLCCK	3BLNC	3INVMK		3FRZE	3FRZE	3PWCLR	3PWCLR	
H	SCASVC	3SCAN1	3XMTAD	3XMTE-	3ENZR	3EP2	3ADAC	3ELNC	3ENBL-		3SVC-	3CFR0-	3CFR2-			
J		3SCAN2	3STRCY	3XMTE-	3REC+	3SR11+	ACDACC	CTWD2	3ENBL-		3GND59	3FR0+	3FR2+	3CFR0+	3CFR2+	
K	3SRSV+	3SNIND	3XMTAD	3FR3+	3IFMC+	3XMT+	BKSL3	3AXNC	3SCAN1	3ZROSR	3FRZE	3EFRC	3GAD61	BAC11	BAC09	
L	3XMT+	3BLCCK	3FR2+	3FRC+	3EXMT	3EP2	3BRKDN	3BLOCK	3SCAN2	3XTRQ+	3PWCLR	3EFR0	3GND61	BAC11	BAC09	
M	3SN2ND	SCAN0+	3CYNC	3CYND	3IFMC+	3RC+	HKSL3	3AXNC	3AXND	3LDFR	3JMP59	3LDFR	3LCFR			
N	SCNSVC	3SN2ND	3FR1+	3CY-	3XTRQ+	3REC+	HBREAK	3REC+	3ENAX-			3FRC+	3FR2+	3LDAUX	3LDAUX	
P		3SCAN1	3CYNC	3LY-	3XMT+	3IFMD+	BTIC	3PARND	3ENAX-	3MBSR	3IFMD-	3FR1+	3FR3+	3CFR1+	3CFR3+	
R		3SCAN2	3FBPC+	3REC+	3HECE-	3ESRSV	3PAR1	3CY+	3RD+	IOP4	3XMT-			3CFR1-	3CFR3-	
S	3SCAN3	3SN2NC	3DYNC	3IFMD+	3RESC-	3XMT+	3RC-	3PARND	3PATY-	3ENAX-	3IFMD+	3CFR1-	3CFR3-			
T	3HERND	3SCAN1	3IFMD+		3CLSE-	3XTRQ+	3REC+		3PARND	3LDAUX	3REC-	3GND60	3GAD61	BAC10	BAC08	
U	HERE*	3SCAN2	3DYNC	3ESRSV	3CARD1	3IFMD+	3CY+		3PAR1		3RSTRT	3GND60	3GND61	BAC10	BAC08	
V		3HERNC			3STRCY		3PATY+					3LDFR	3LCFR			

TABLE II-19.

PANEL 5 ... PORT 3/LINE ADAPTOR 4

	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16	
	W2C1C	EIAR	R111	W501	R111	ROC1	R3C2	R111	R201	R2C5	R205	R205	R2C5	R205	R2C1	R205	
A																	A
B																	B
C		4GND02		4GND04			4GND06									4GND14	C
D	4SDB	4GND02	4RD+	4SRCK	4SCBF+	4REC-		4RECE-		4SHIFT	4SHIFT	4SHIFT	4SHIFT	4SHIFT		4SHIFT	D
E	4RCB	4RINGB	4REC+		4LINE+	4OTNJ1	4RQSO+		4SHIFT	4SR01-	4SR03-	4SR05-	4SR07-	4SR09-	4SHIFT	4SDBF+	E
F	4RSB			4SRCK	4CTNC1	4REC-	4GND06		4RD+	4ZERSR	4ZERSR	4ZERSR	4ZERSR	4ZERSR	4SR10+		F
H	4CSDB	4RING	4RD-		4CLT1	4OTND2		4REC+		BMB01	BMB03	BMB05	BMB07	BMB09		4GND14	H
J	4SRCB	4RING	4RD-		4CLT1	4REC-	4A06JK			4SR01+	4SR03+	4SR05+	4SR07+	4SR09+			J
K	4TRDYB	4GND02	4OLST+		4PTBF+	4RSND	4A06JK	4XMTE-	4ZRDSR	4SR00-	4SR02-	4SR04-	4SR06-	4SR08-	4ZERSR	4SR11+	K
L	4RINGB	4CSDB		4GND04	4LINE-				4SR00+	4SR00+	4SR02+	4SR04+	4SR06+	4SR08+	4SR11+	4SR11-	L
M	4CCETE	4DELAY		4L04	4CTN02		4BFIX		4SR00-	4MBSR	4MBSR	4MBSR	4MBSR	4MBSR	4SR11-	4FRZE	M
N		4CS+	DTALST	4L04	4CLT1		4IFMO+	4XMT+		4SHIFT	4SHIFT	4SHIFT	4SHIFT	4SHIFT		4SHIFT	N
P	4SCTB	4CS+					4REC-		4SHIFT	4SR02+	4SR04+	4SR06+	4SR08+	4SR10+	4SHIFT	4PATY+	P
R	4SCRB	4GND02	4BFIX	4SCRB	4XMT-				4RD-	4SR02-	4SR04-	4SR06-	4SR08-	4SR10-	4SR10-	4PATY-	R
S		4SRDB			4XTFC+		4A06ST		4MBSR	BMB02	BMB04	BMB06	BMB08	BMB10	4MBSR	4GND14	S
T					4RSNO		4A06ST		BMB10	4SR01-	4SR03-	4SR05-	4SR07-	4SR09-	BMB11	4EP2	T
U		4STRDY	4DELAY		4RS1					4SR01+	4SR03+	4SR05+	4SR07+	4SR09+		4EP2	U
V	4HERE	4STRDY			4RS1		4BR1			4MBSR	4MBSR	4MBSR	4MBSR	4MBSR		4ZRDSR	V

	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16	
	W602	EIAR	W602	W501	W501	R202	R602	R602	R602	R602	R202	R107	R107	R121	R111	R002	
A																	A
B																	B
C		4GND34		4GND36							4GND43						C
D	4JLT1	4GND34	4SCTE	4SCK	4CCTD		4JMP39	4JMP40	4JMP41		4SRSV+	4CARDT	4BRENB	4IOPCS	4ENDI	4SR00-	D
E		4RDB			4CDT			4FR3+			4RSYN-	4COTO	4BR1	4EBPC+	4BRENB	4SR01-	E
F	4SCB		4SCTB	4SCK	4CCTO	4PWCLR		4EXMT			4PWCLR	4DY+	BKRC4	4DTSY+		4DSYND	F
H	4RCSO+	4RDBI				4REC-	4CLOCK	4BRKON		4CLOCK	4RSYN-	4DY-	4BKRC+	4F1	4CHRDN	4SRC2-	H
J		4RDBI				4REC+	4DTSY-	4ENZR		4SYNC-	4RSYN+	4STCK	4ENAX+	4IFMD-	4CHRDN	4SR03+	J
K	4RSB	4GND34			4L37	4SRCK	4ZERSR	4ZROSR	4PWCLR	4START	4SRSV-	4SCK	4ENAX-	4DTSY-	4IFMD-	4CSYND	K
L	4TMRO+	4COETB		4GND36	4L37	4RECE-	4ZROSR	4START	BPCLR		4REC-	4RD+	4ENBL+	4ESFT	4REC+	4SR04-	L
M				4L36	4L37		4JMP35	4JMP40	4JMP41			4RDBI	4ENBL-	4DY-	4DSYND	4SR05+	M
N	4TRDYB	4COT		4L36	4L37						4START	4DTSY+	4ENDI	4SVC-	4DTSY-	4DSYND	N
P	4V+BC1	4CDT	4V+BC3				4STCK				4GN043	4DTSY-	4ENO	4IDPCS	4DTSY-	4SR06+	P
R	4V-BC1		4V-BC3	4SCTB	4JP37	4PWCLR	4XMT-				4PWCLR	4CS-	4HEREB	4EFRO		4SR07-	R
S	4V+BC1		4V+BC3		4CCT	4XMT-	4SRCK	4CLOCK	4BRKON		4SYNC-	4CS+	4HERE	4F1		4DSYND	S
T					4JM37	4XMT+	4REC-	4ESFT	4EXMT				4BLOCK	4SVC-		4HEREB	T
U						4STCK	4CLOCK	4SHIFT	4MBSR	4END	4CLOCK		BKSLB	4IOPCS		4BLOCK	U
V	4V-B01		4V-BC3			4XMTE-				4FR3+	4SVC-				4ENDI	4HERND	V

TABLE II-20.

PANEL 5 ... PORT 3/LINE ADAPTOR 4

	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32	
	R202	R123	R123	R201	R201	R201	R205	R205	R205	R205	R123	R123	6994	R123	R111		
A																	A
B																	B
C					4GND19	4GND20											C
D	4FR3+	4SR00+	4SR06+				4INVMK	4INVMK	4STCK	4BRKDN	4SRSV+	4EBPC+	SCAN1+	4CFR3+	4ADR08		D
E	4DY-	4SR01+	4SR07+	4INVMK	4ACAC	4START			4CLSD-	4RQSD-	4DLST+	4IFMD+	SCAN1-	4CFR2+	BKSL4		E
F		BKSL4	BKSL4	BACC7	4GND19	4GND20	4PWCLR	4PWCLR	4PWCLR	4PWCLR	4ENBL+	4ENBL+	SCAN2+	4ENAX+			F
H	4LINE-	DABT00	DABT06	4REC-				4PAR1		4RS1	EAC00	EAC06	SCAN2-	EAC08	DIAD08		H
J	4LINE+	DABT01	DABT07	4XMT+			4EBPC+	4PAR+	4CLSD+	4RQSD+	EAC01	EAC07	SCAN3+	EAC09			J
K	4CLOCK	4SR02+	4SR08+	4PWCLR	4PWCLR	4PWCLR	BACC6	EAC02	4CS-	4XTRQ-	4PAR+	4STRDY	SCAN3-	4CFR1+	4ADR09		K
L	4LINE+	4SR03+	4SR09+	4IFPD+	4BRKG+		BACC6	BAC02	4CS+	4XTRQ+	4RQSD+	4TMRD+	4SCAN1	4CFR0+	BKSL4		L
M	4FRZE	BKSL4	BKSL4	4IFPD-		4SVC-		4CLOCK		ET1	4ENBL+	4ENBL+	4SCAN2	4ENAX+			M
N	4FR3+	DABT02	DABT08			4RSTRT	4INVMK	4INVMK	4INVMK	4INVMK	EAC02	EAC08	4SCAN3	EAC10	DIAD09		N
P	4PATY-	DABT03	DABT09	4INVMK	4FR3+	4REC-	4TMRD+	4CLST+	4SRSV+	4XTRQ+	EAC03	EAC09	4ADR08	EAC11			P
R		4SR04+	4SR10+	BAC07	4IFPD-	4XMT+			4SRSV-	4XTRQ-	4XTRQ+	4RING	4ADR09	4RQSD+	4ADR10		R
S	4PTBF+	4SR05+	4SR11+	4CLOCK	4START	4XMT-		4SRSV-	4ESRSV		4CLSD+	4CARDT	4ADR10	4RQSD+	BKSL4		S
T		BKSL4	BKSL4	4CTSY-	4XMT-	4REC+	BACTY	BAC01	BAC00	BAC04	4ENBL+	4ENBL+		BKSL4			T
U	4FR3+	DABT04	DABT10	4XMT-			BACTY	EAC01	BAC00	BAC04	EAC04	EAC10		DIAD11	DIAD10		U
V	4PATY+	DABT05	DABT11	4REC+				4CHRDN	4CHRDN		EAC05	EAC11		DICTL			V

	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32	
	R111	R002	R001	R111	R121	R121	R121	R001	R111	R603	R602	R205	R205	R205	R205		
A																	A
B																	B
C											4GND59	4GND60	4GND61				C
D	4SRSV+	4BLOCK	4TMRD+	4RQSD+		4EP2		CTWD1	4SCAN1	IOP4	4JMP59	4CLOCK	4FR1+	4LDAUX	4LDAUX		D
E	4RSYN+	SCAN0-	4XMTND	4CLSD+		4RD+		4BLNC	4SCAN2	4ENBL-				4CFR0-	4CFR2-		E
F	4SNIND	4SNIND	4CARCT	4XMTND		4DTSY+		4BLOCK	4BLND	4INVMK		4FRZE	4FRZE	4PWCLR	4PWCLR		F
H	SCNSVC	4SCAN1	4XMTND	4XMTE-	4ENZR	4EP2	4ADAC	4BLNC	4ENBL-		4SVC-	4CFR0-	4CFR2-				H
J		4SCAN2	4STRDY	4XMTE-	4REC+	4SH11+	ADDACC	CTWD2	4ENBL-		4GND59	4FR0+	4FR2+	4CFR0+	4CFR2+		J
K	4SRSV+	4SNINC	4XMTND	4FR3+	4IFPD+	4XMT+	BKSL4	4AXND	4SCAN1	4ZROSR	4FRZE	4EFR0	4GND61	BAC11	BAC09		K
L	4XMT+	4BLOCK	4FR2+	4FR0+	4EXMT	4EP2	4BRKDN	4BLOCK	4SCAN2	4XTRQ+	4PWCLR	4EFR0	4GND61	BAC11	BAC09		L
M	4SN2ND	SCAN0+	4DYNC	4DYND	4IFPD+	4RD+	BKSL4	4AXND	4AXND	4LDFR	4JMP59	4LDFR	4LDFR				M
N	SCNSVC	4SN2ND	4FR1+	4DY-	4XTRQ+	4RFC+	HBREAK	4RFC+	4ENAX-			4FR0+	4FR2+	4LDAUX	4LDAUX		N
P		4SCAN1	4DYNC	4DY-	4XMT+	4IFMD+	BTIC	4PARND	4ENAX-	4MBSR	4IFMD-	4FR1+	4FR3+	4CFR1+	4CFR3+		P
R		4SCAN2	4EBPC+	4REL+	4RECE-	4ESRSV	4PAR1	4DY+	4RD+	IOP4	4XMT-			4CFR1-	4CFR3-		R
S	4SCAN3	4SN2ND	4DYRC	4IFMD+	4RQSC-	4XMT+	4RD-	4PARND	4PATY-	4ENAX-	4IFMD+	4CFR1-	4CFR3-				S
T	4HERND	4SCAN1	4IFMD+		4CLSD-	4XTRQ+	4REC+		4PARND	4LDAUX	4REC-	4GND60	4GND61	BAC10	BAC08		T
U	HERE+	4SCAN2	4DYNC	4ESRSV	4CARDT	4IFMD+	4DY+		4PAR1		4RSTRT	4GND60	4GND61	BAC10	BAC08		U
V		4HERND			4STRDY		4PATY+					4LDFR	4LDFR				V

TABLE II-21.

APPENDIX III

PDP-8/201A LINE ADAPTOR INTERFACE
FOR USE WITH A
PDP-8 WITHOUT USING THE DATA-BREAK FACILITY

APPENDIX III

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PDP-8/201A LINE ADAPTOR INTERFACE
FOR USE WITH A
PDP-8 WITHOUT USING THE DATA-BREAK FACILITY

The only difference between this version of the 201A communication adaptor and the basic 201A communication adaptor presented in Appendix I is that it uses a character buffer internal to the 201A line adaptor interface instead of using the data break facility and PDP-8 core buffers. This necessitates the addition of control circuitry to transfer characters between the SDR register and this internal buffer (BUF) and additional micro-instructions to read, write, and clear BUF. The additional device code for the set of IOTs is taken to be the fourth in the set used by 201A communication adaptor (see Programming and Control Considerations).

This set of IOTs is defined as follows:

Read Character Buffer (6XX1)

This micro-instruction causes the contents of the 201A line adaptor character buffer to be logically ORed to the accumulator.

Clear Character Buffer (6XX2)

This micro-instruction causes the 201A line adaptor character buffer to be cleared.

Write Character Buffer (6XX4)

This micro-instruction causes the contents of the PDP-8 accumulator to be loaded into the 201A line adaptor character buffer (BUF).

In order to use the same basic 201A line adaptor, the data break control signals were simulated, except that the transfer is to and from BUF instead of core. The remainder of the Appendix presents the detailed logic circuits with a brief description of their function.

Pseudo Data-Break Control (Diagram III-1)

Through the #BKRQ flip-flop, the line adaptor initiates the transfer to or from the SDR register from or to the BUF register. When #BKRQ is set, the direction of transfer is specified by the DICTL signal. The #BKRQ flip-flop is cleared by the first BT1 pulse after it is set. The next BT1 pulse is used to generate the #BRKDN signal which causes the reading or strobing of the BUF register. The #BRKQ flip-flop is set each time the frame counter overflows while in the text state and when the line adaptor first enters the transmit state to fetch the first character to be transmitted. All of the logic in Diagram III-1 is in Bay 2 of the interface.

Control Gating (Diagram III-2)

The PDP-8's address-accepted signal is simulated by the ADRAC flip-flop, and the buffered-break signal is effected by the BBRK flip-flop. The sequencing through the states effected by BBRK and ADRAC is accomplished by the BT1, and BT2 pulses. The BUF register is cleared by a PDP-8 power clear signal, an explicit IOT, and by the interface before it loads the SDR register into it. The signal used to load the SDR register into BUF is READ, while LOAD is generated by the IOT used to write or load BUF from the PDP-8 accumulator.

BUF Register (Diagram III-3)

Diagram III-3 shows the internal buffer register.

BUF Gating (Diagram III-4)

Diagram III-4 shows the drivers and control gating necessary to load the BUF register into the PDP-8 accumulator.

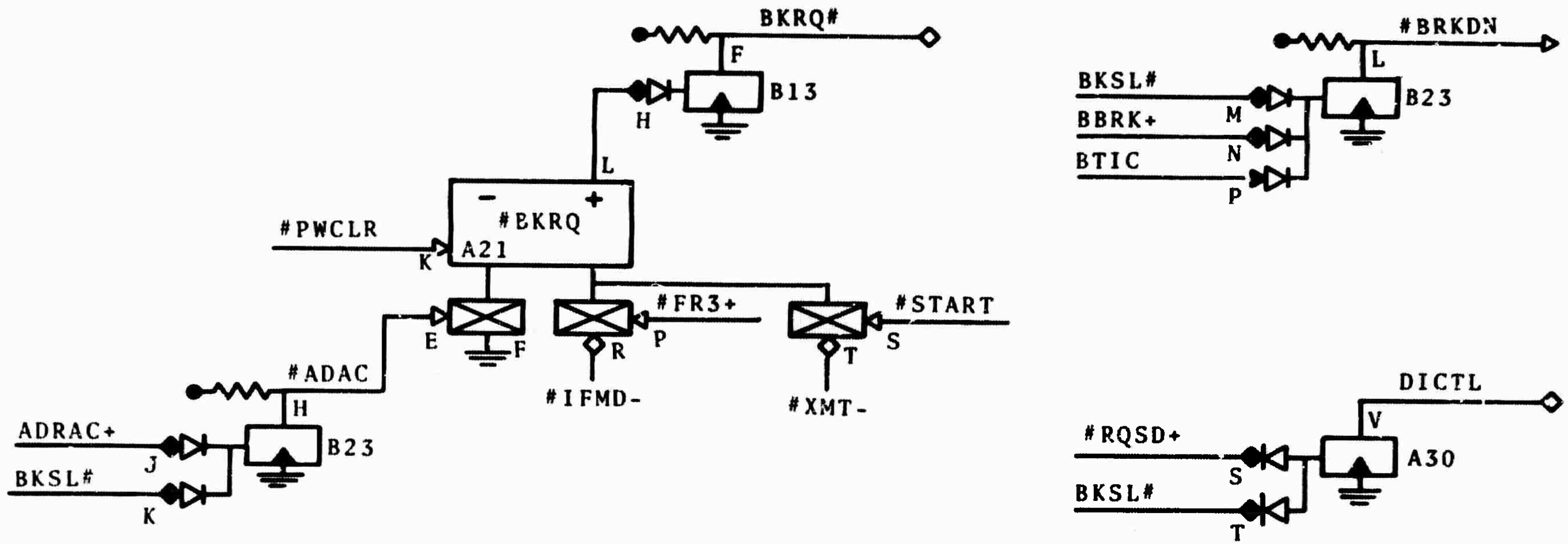

Diagram III-1. PSEUDO DATA BREAK CONTROL

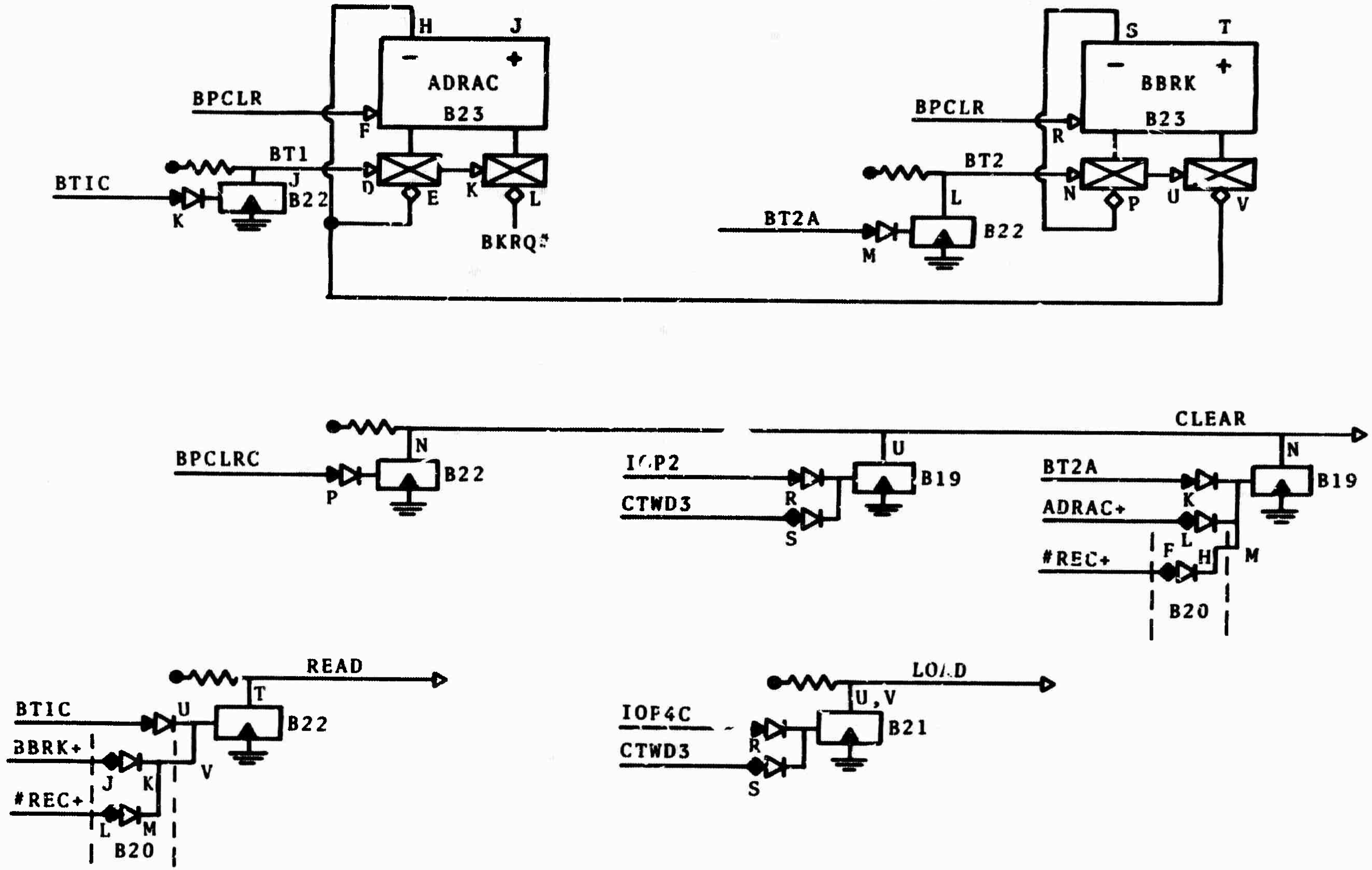

Diagram III-2. CONTROL GATING

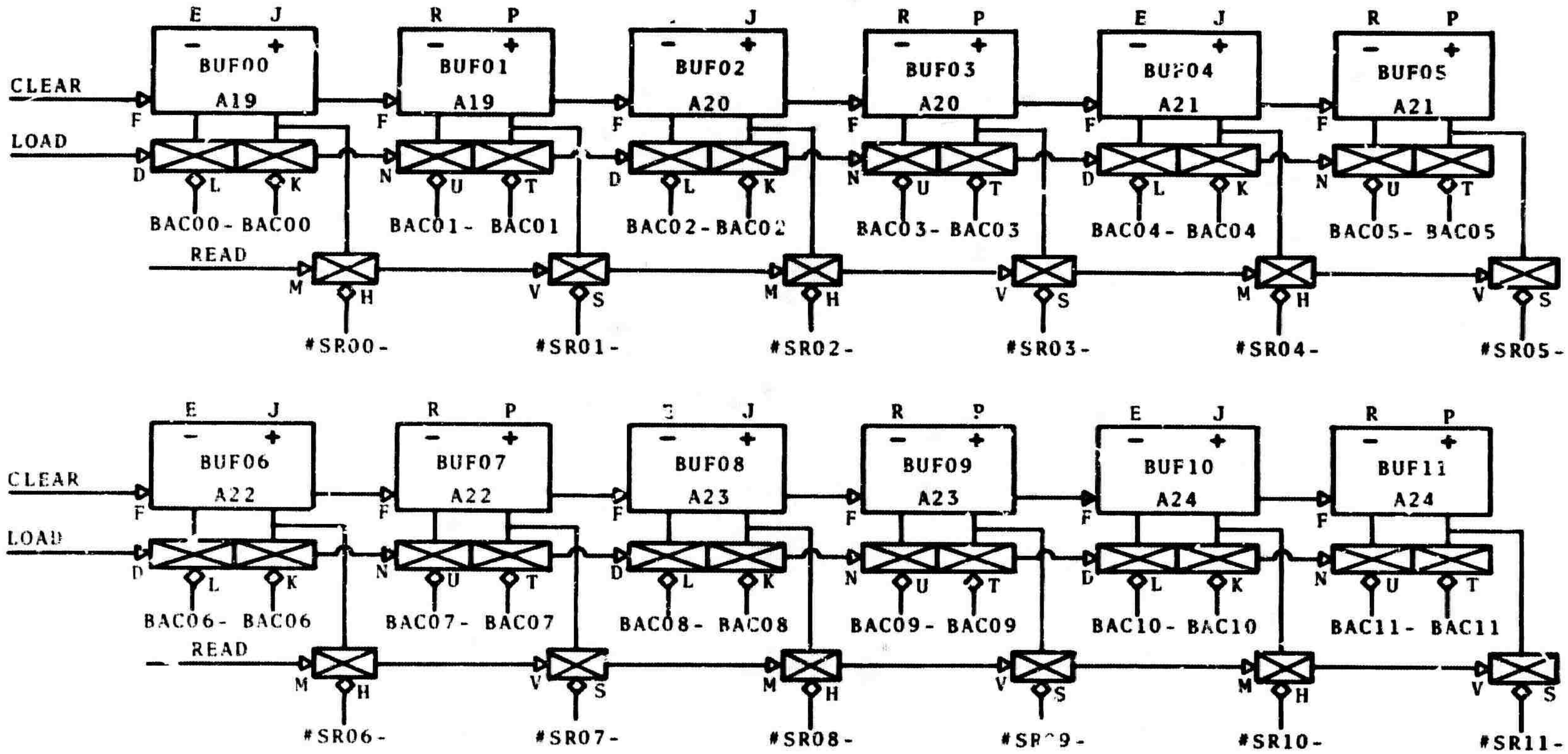

Diagram III-3. BUF REGISTER

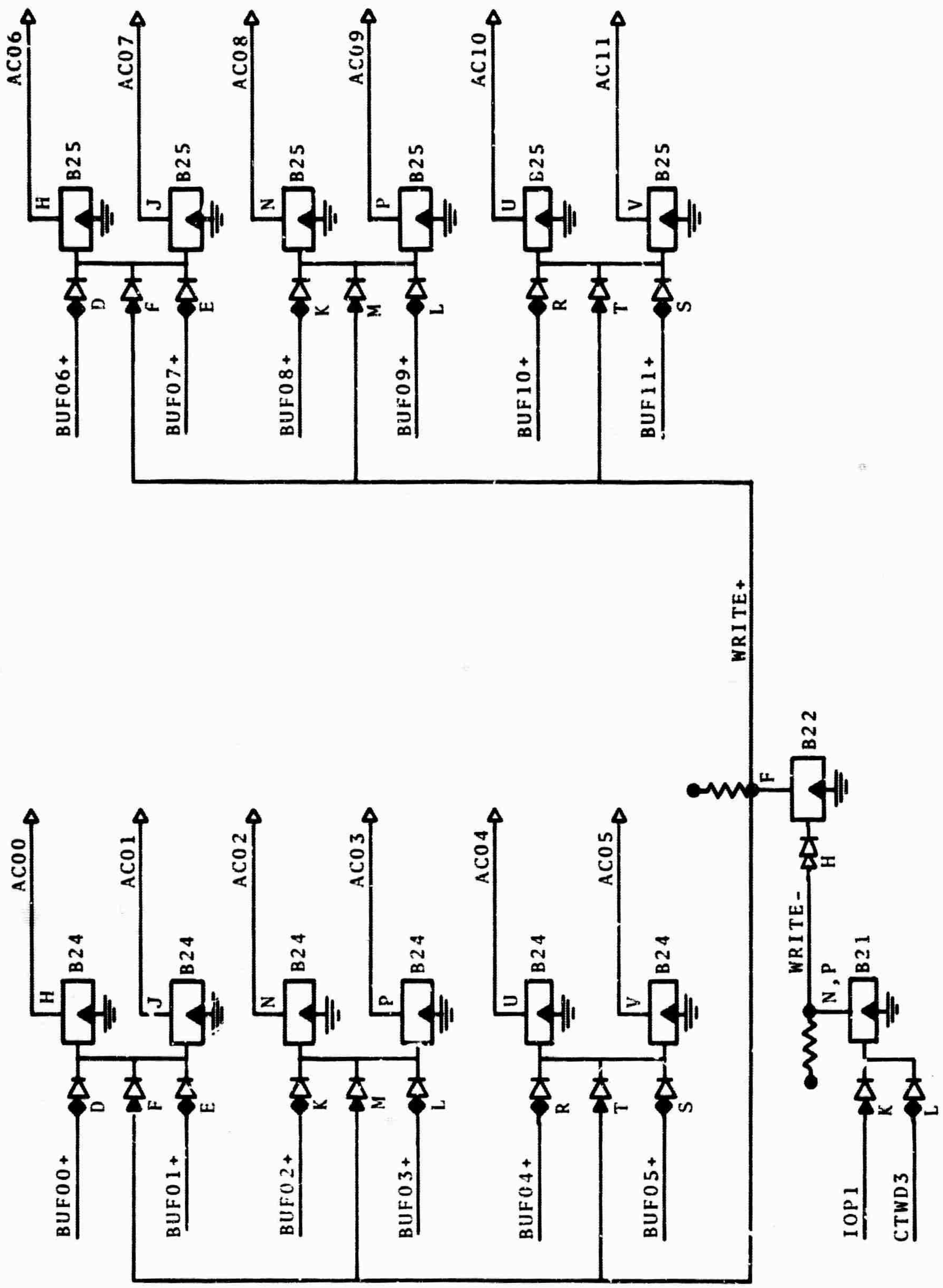

Diagram III-4. BUF GATING

<u>SDR Register</u> (Diagram III-5)

Diagram III-5 is a revision of Diagram 1, described in the report, to reflect the loading of the SDR register from BUF instead from the buffered memory buffer.

<u>Device Select Code</u> (Diagram III-6)

The device select code is a two octal digit number which selects an external device during an input/output operation. The device code appears in positions 3 through 8 of the memory buffer during an IOT instruction, alerting the external device when it is being selected.

This version of the 201A L.A. has associated with it four separate device codes as discussed above. In order to specify the four devices it is sufficient, because of the aforementioned requirements, to define only a four-bit number which appears in positions 3-6 of the M.B. during an IOT instruction. This number must also be realized in the hardware, and this is accomplished via an R002 diode module.

Thus to specify the desired set of devices codes the appropriate diodes are removed. For example, using the set 40,41,42,43, as before, the diodes connected to pins E, H, L, and P must be removed.

The remainder of Diagram III-6 shows the gating necessary to obtain the signals to identify each of the devices.

<u>Device Selection Gating</u> (Diagram III-7)

The gates shown in Diagram III-7 are located in Bay 2 and provide the signals to differentiate between Control Word 1 and Control Word 2 operation.

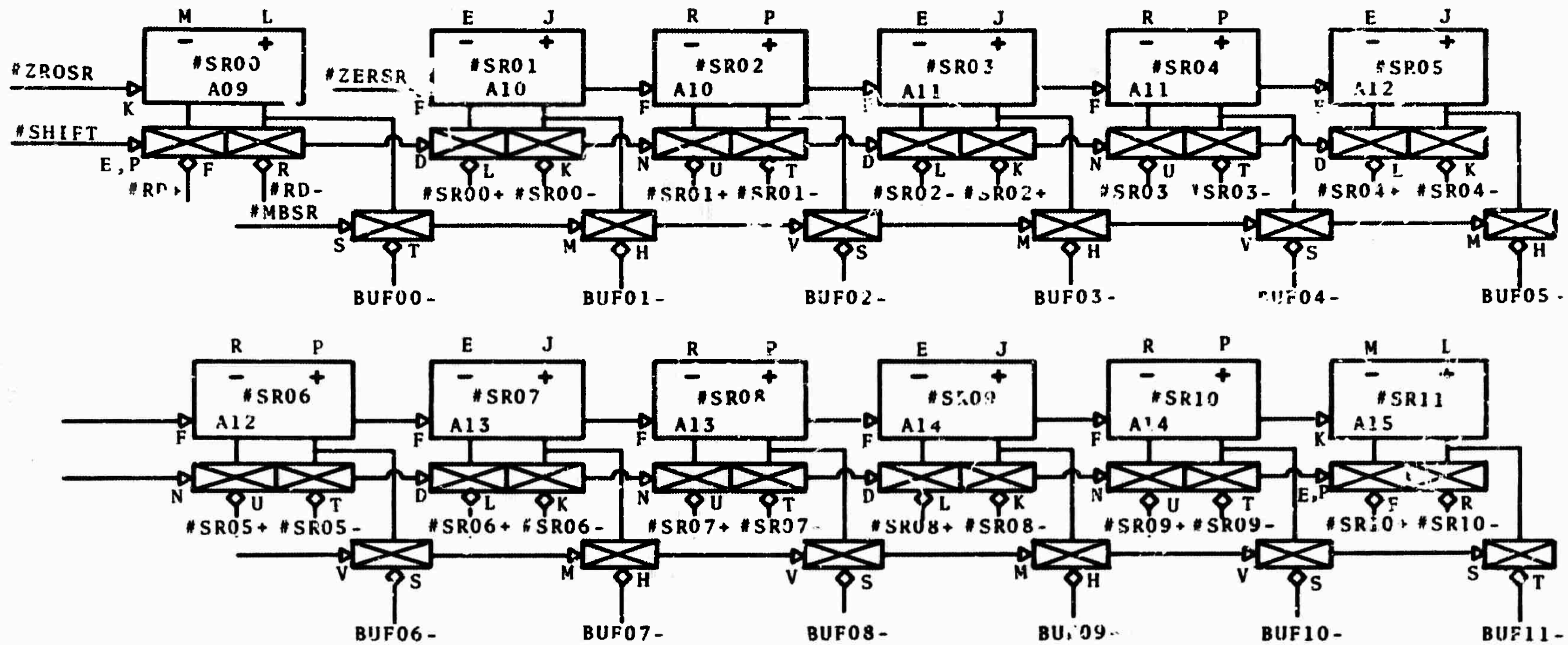

Diagram III-5. SDR REGISTER

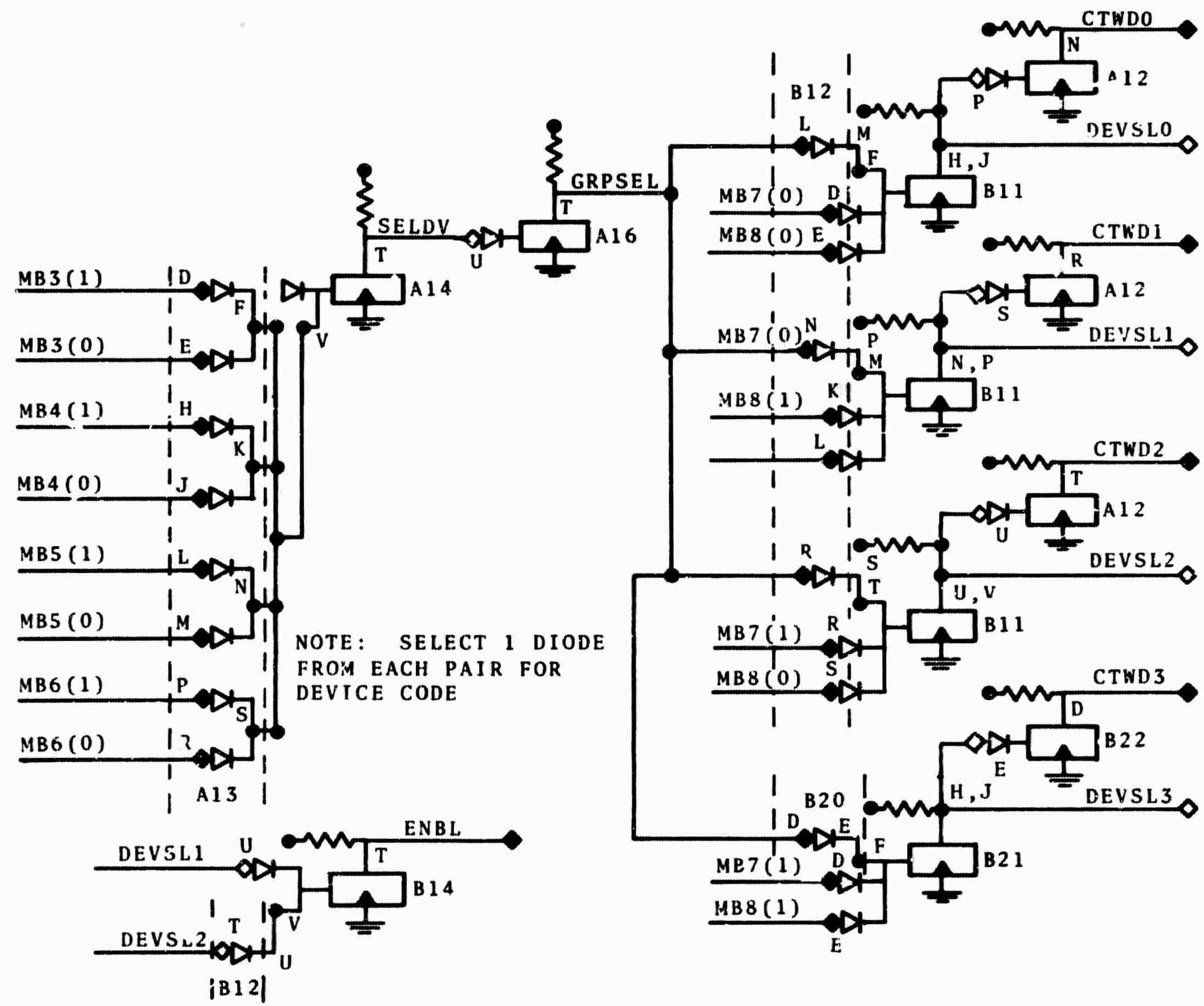

Diagram III-6. DEVICE SELECT CODE

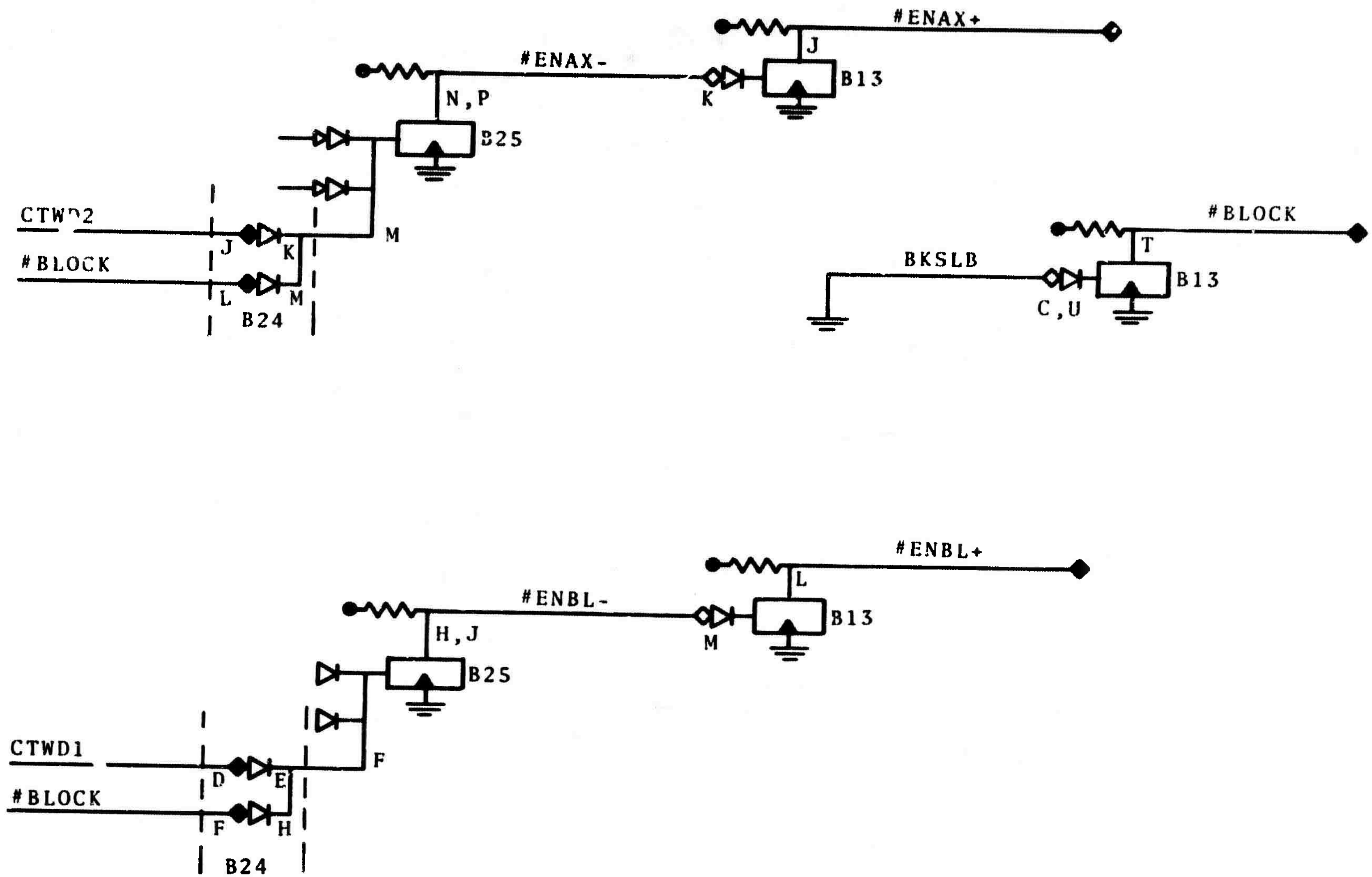

Diagram III-7. DEVICE SELECTION GATING

Interrupt Control (Diagram III-8)

Every time a character is transferred between the 201A L.A. and the BUF register, a character service flag (#SRSV) is set, as described before.

This flag in turn sets the appropriate flag, transmit (XINT) or receive (RINT), which causes an interrupt request. If interrupts are enabled in the PDP-8, a program interrupt is generated. Via the appropriate IOT micro-instruction, the program can identify the device causing the interrupt. The SKIP signal will be generated and a program skip forced if this IOT is executed. It is the program's responsibility to clear the interrupt after it is identified, and the remainder of the gates allow for this.

Extended Accumulator Control (Diagram III-9)

In order to provide the IOT structure described under Programming and Control Considerations, the extended accumulation (EAC) buss was implemented. The full power of the EAC is not realized until there are multiple devices using the buss, since it provides the mechansim for multiple inputs to the PDP-8 AC. Diagram III-9 shows the gating necessary to generate the SKIP signal on a skip under mask IOT.

Accumulator Input Gating (Diagram III-10)

Diagram III-10 shows the buffers which gate the EAC buss onto the AC buss. For other devices to use the EAC buss, they need provide only the appropriate input to the ENBL gate and the gates for the EAC buss.

Extended Accumulator Buffers (Diagram III-11)

Diagram III-11 shows a set of buffers necessary to accomplish the inversion to gate the EAC onto the AC. The clamped loads for the EAC buss are also indicated.

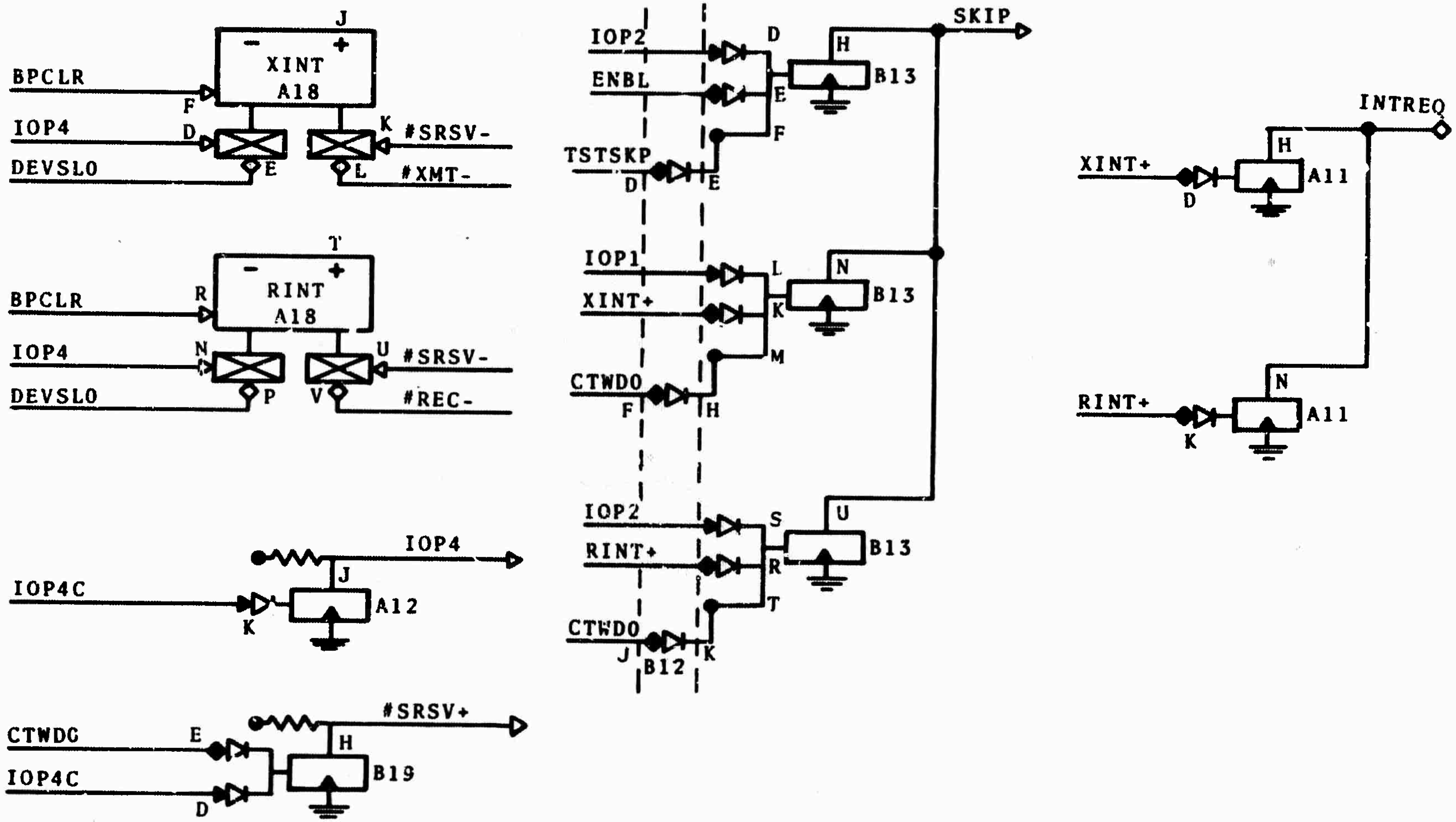

Diagram III-8. INTERRUPT CONTROL

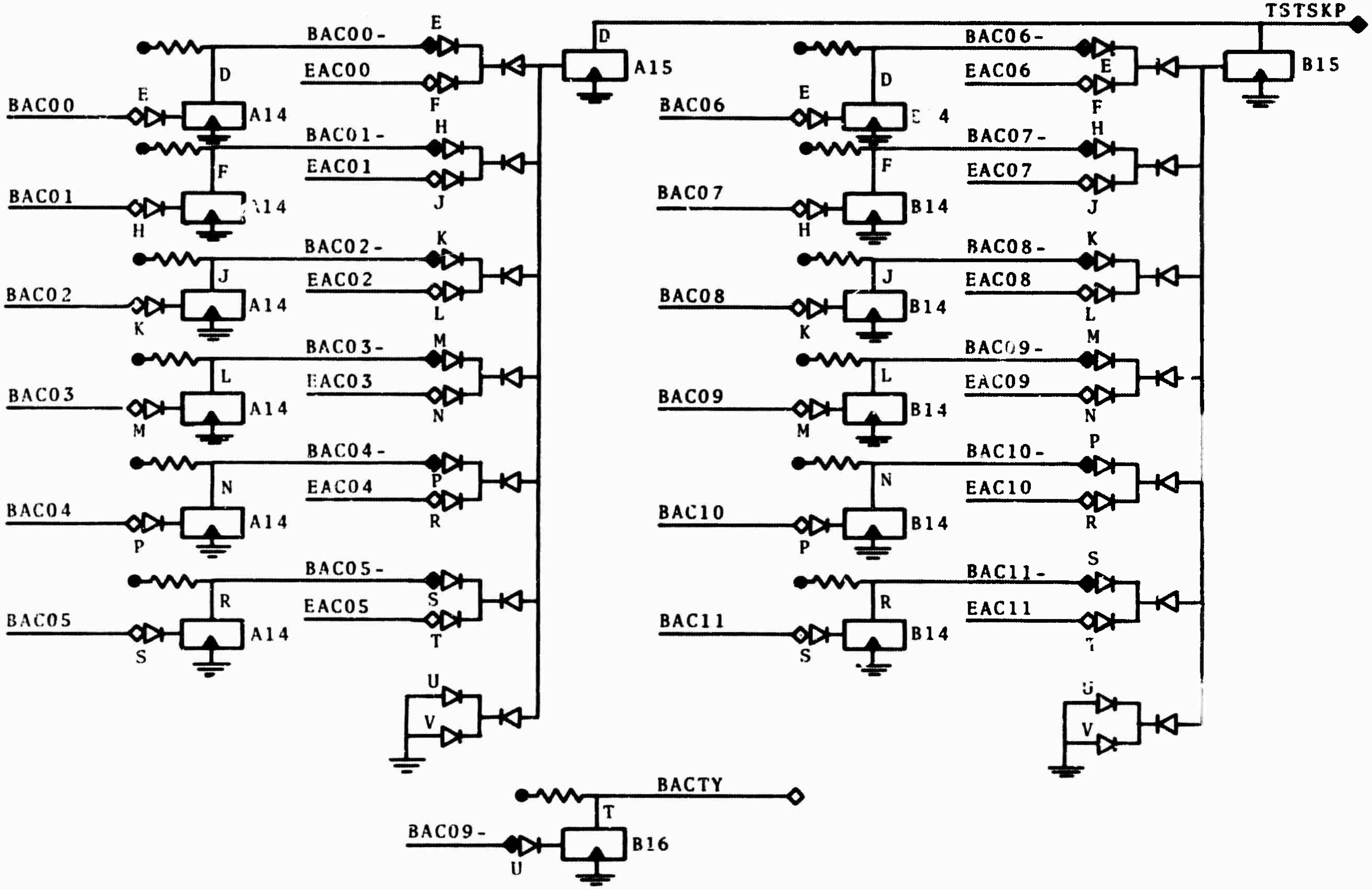

Diagram III-9. EXTENDED ACCUMULATOR CONTROL

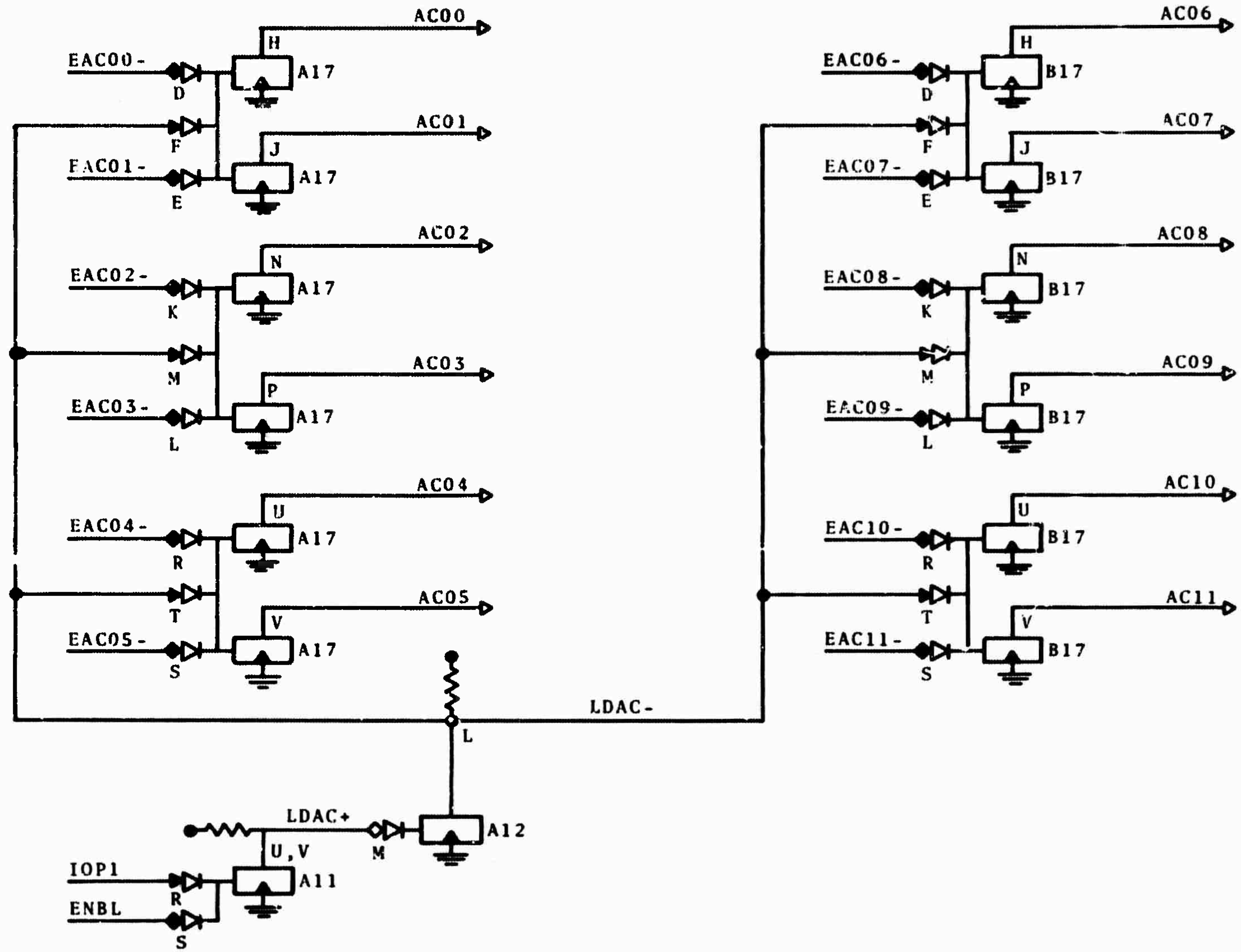

Diagram III-10. ACCUMULATOR INPUT GATING

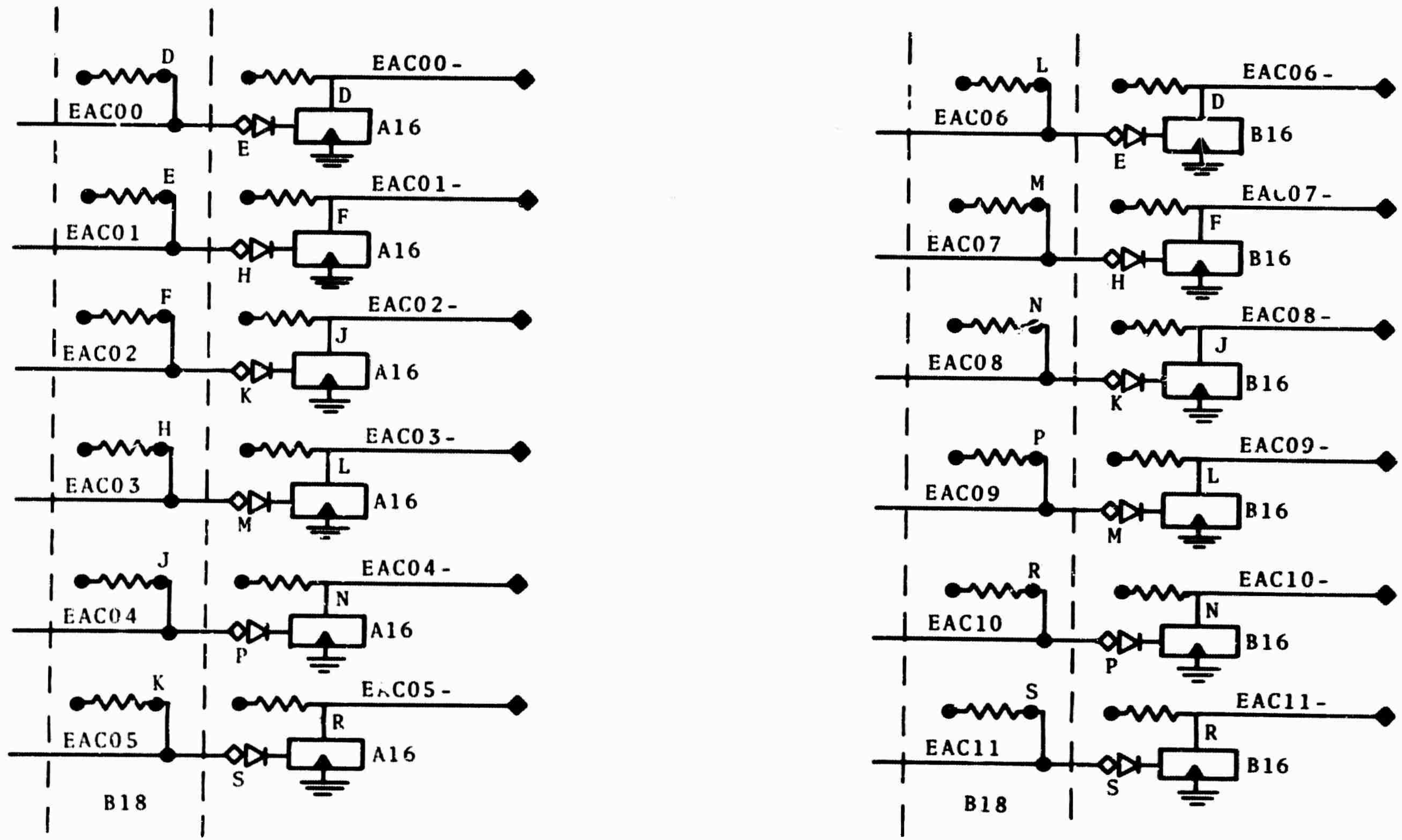

Diagram III-11. EXTENDED ACCUMULATOR BUFFERS

Miscellaneous Circuits (Diagram III-12)

Diagram III-12 is best described as the left-over circuits without a logical home.

Cable Layout (Diagram III-13)

The input/output cables for this version of the 201A line adaptor are shown in Diagram III-13. The correspondence between signal names, module positions, and pin connections for the 201A line adaptor and the PDP-8 are given in Tables III-1 through III-4.

Module Utilization (Tables III-5 through III-8)

Tables III-5 through III-8 give the module utilization for this version of the 201A line adaptor. In addition to the module utilization, a complete signal name map is also shown (Tables III-5 through III-8).

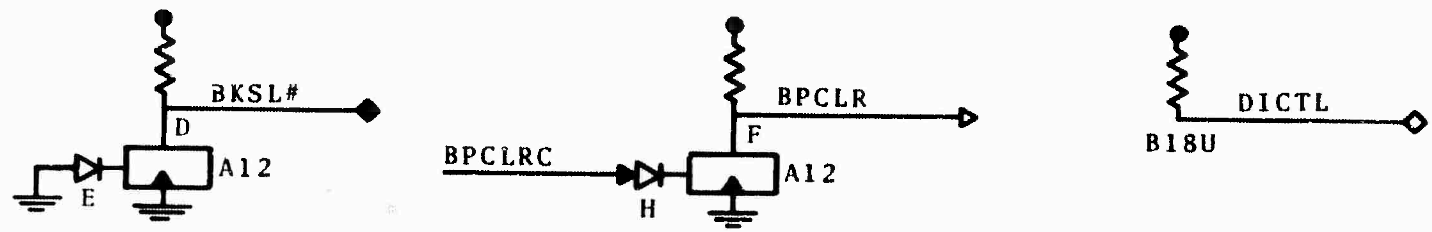

Diagram III-12. MISCELLANEOUS CIRCUITS

'A'

	01 02	03 04	05 06
D	BAC00	BMB00	AC00
E	BAC01	BMB01	AC01
F			
H	BAC02	BMB02	AC02
J			
K	BAC03	BMB03-	AC03
L			
M	BAC04	BMB03	AC04
N			
P	BAC05	BMB04-	AC05
R			
S	BAC06	BMB04	AC06
T	BAC07	BMB05-	AC07
U			
V	BAC08	BMB05	AC08

'B'

	01 02	03 04	05 06
D	BAC09	BMB06-	AC09
E	BAC10	BMB06	AC10
F			
H	BAC11	BMB07-	AC11
J			
K	IOP1	BMB07	SKIP
L			
M	IOP2	BMB08-	INTREQ
N			
P	IOP4C	BMB08	--
R			
S	BT1C	BMB09	--
T	BT2A	BMB10	--
U			
V	BPCLRC	BMB11	--

Diagram III-13. CABLE LAYOUT

TABLE III-1

BUFFERED ACCUMULATOR OUTPUTS

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A01D, A02D	BAC00			BAC0	ME34D
A01E, A02E	BAC01			BAC1	ME34E
A01H, A02H	BAC02			BAC2	ME34H
A01K, A02K	BAC03			BAC3	ME34K
A01M, A02M	BAC04			BAC4	ME34M
A01P, A02P	BAC05			BAC5	ME34P
A01S, A02S	BAC06			BAC6	ME34S
A01T, A02T	BAC07			BAC7	ME34T
A01V, A02V	BAC08			BAC8	ME34V
B01D, B02D	BAC09			BAC9	MF34D
B01E, B02E	BAC10			BAC10	MF34E
B01H, B02H	BAC11			BAC11	MF34H

TABLE III-2

ACCUMULATOR INPUTS

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A05D, A06D	AC00	*	*	AC0	PE2D
A05E, A06E	AC01	*	*	AC1	PE2E
A05H, A06H	AC02	*	*	AC2	PE2H
A05K, A06K	AC03	*	*	AC3	PE2K
A05M, A06M	AC04	*	*	AC4	PE2M
A05P, A06P	AC05	*	*	AC5	PE2P
A05S, A06S	AC06	*	*	AC6	PE2S
A05T, A06T	AC07	*	*	AC7	PE2T
A05V, A06V	AC08	*	*	AC8	PE2V
B05D, B06D	AC09	*	*	AC9	PF2D
B05E, B06E	AC10	*	*	AC10	PF2E
B05H, B06H	AC11	*	*	AC11	PF2H

*Note: Collector of Grounded-Emitter Transistor

TABLE III-3

TIMING CONTROL SIGNALS

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B01S, B02S	BT1C	→	→	BT1	MF34S
B01T, B02T	BT2A	→	→	BT2A	MF34T
B01V, B02V	BPCLRC	→	→	B POWER CLEAR	MF34V

TABLE III-4

PROGRAMMED INPUT/OUTPUT CONTROL

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B05M, B06M	INTREQ	*1	*1	INTERRUPT REQUEST	PF2M
B05K, B06K	SKIP	*1	*1	SKIP	PF2K
B01K, B02K	IOP1			IOP1	MF34K
B01M, B02M	IOP2			IOP2	MF34M
B01P, B02P	IOP4C			IOP4	MF34P

*Note: Collector of Grounded-Emitter Transistor.

PANEL 1 ... COMMON SECTION (WITHOUT DATA BREAK)

	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16	
	W021	W021	W021	W021	W021	W021					R111	R1D7	R0D2	R107	R141	R1D7	
A																	A
B																	B
C												GNDA12			GNDA15		C
D	BAC00	BAC00	BMB00	BMB00	AC00	AC00					XINT+	BKSL#	BMB03-	BAC00-	TSTSKP	EAC00-	D
E	BAC01	BAC01	BMB01	BMB01	AC01	AC01						GNDA12	BMB03	BAC00	BAC00-	EAC00	E
F												BPCLR	SELND	BAC01-	EAC00	EAC01-	F
H	BAC02	BAC02	BMB02	BMB02	AC02	AC02					INTREQ	BPCLRC	BMB04-	BAC01	BAC01-	EAC01	H
J												IOP4	BMB04	BAC02-	EAC01	EAC02-	J
K	BAC03	BAC03	BMB03-	BMB03-	AC03	AC03					RINT+	IOP4C	SELND	BAC02	BAC02-	EAC02	K
L												LDAC-	BMB05-	BAC03-	EAC02	EAC03-	L
M	BAC04	BAC04	BMB03	BMB03	AC04	AC04						LDAC+	BMB05	BAC03	BAC03-	EAC03	M
N											INTREQ	CTWD0	SELND	BAC04-	EAC03	EAC04-	N
P	BAC05	BAC05	BMB04-	BMB04-	AC05	AC05						DEVSL0	[illegible]	BAC04	BAC04-	EAC04	P
R											IOP1	CTWD1	BMB05	BAC05-	EAC04	EAC05-	R
S	BAC06	BAC06	BMB04	BMB04	AC06	AC06					ENBL	DEVSL1	SELND	BAC05	BAC05-	EAC05	S
T	BAC07	BAC07	BMB05-	BMB05-	AC07	AC07						CTWD2		SELDV	EAC05	GRPSEL	T
U											LDAC+	DEVSL2			GNDA15	SELDV	U
V	BAC08	BAC08	BMB05	BMB05	AC08	AC08					LDAC+			SELNO	GNDA15		V

	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16	
	W021	W021	W021	W021	W021	W021					R111	R001	R111	R1D7	R141	R1D7	
A																	A
B																	B
C															GNDB15		C
D	BAC09	BAC09	BMB06-	BMB06-	AC09	AC09					BMB07	TSTSKP	IOP2	BAC06-	TSTSKP	EAC06-	D
E	BAC10	BAC10	BMB06	BMB06	AC10	AC10					BMB08	SKIP1	ENBL	BAC06	BAC06-	EAC06	E
F											DEVND0	CTWD0	SKIP1	BAC07-	EAC06	EAC07-	F
H	BAC11	BAC11	BMB07-	BMB07-	AC11	AC11					DEVSL0	SKIP2	SKIP	BAC07	BAC07-	EAC07	H
J											DEVSL0	CTWD0		BAC08-	EAC07	EAC08-	J
K	IOP1	IOP1	BMB07	BMB07	SKIP	SKIP					BMB07	SKIP3	XINT+	BAC08	BAC08-	EAC08	K
L											BMB08-	GRPSEL	IOP1	BAC09-	EAC08	EAC09-	L
M	IOP2	IOP2	BMB08-	BMB08-	INTREQ	INTREQ					DEVND1	DEVND0	SKIP2	BAC09	BAC09-	EAC09	M
N											DEVSL1	GRPSEL	SKIP	BAC10-	EAC09	EAC10-	N
P	IOP4C	IOP4C	BMB08	BMB08							DEVSL1	DEVND1		BAC10	BAC10-	EAC10	P
R											BMB07-	GRPSEL	RINT+	BAC11-	EAC10	EAC11-	R
S	BT1C	BT1C	BMB09	BMB09							BMB08	DEVND2	IOP2	BAC11	BAC11-	EAC11	S
T	BT2A	BT2A	BMB10	BMB10							DEVND2	DEVSL2	SKIP3	ENBL	EAC11	BACTY	T
U											DEVSL2	ENBLND	SKIP	DEVSL1	GNDB15	BAC09-	U
V	BPCLRC	BPCLRC	BMB11	BMB11							DEVSL2			ENBLND	GNDB15		V

TABLE III-5.

PANEL 1 ... COMMON SECTION (WITHOUT DATA BREAK)

	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32
	R123	R202	R205	R205	R205	R205	R205	R205				W050S				
A																
B																
C																
D	FAC00-	IOP4	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD				#XMT+				
E	FAC01-	DEVSLO	BUF0D-	BUF02-	BUF04-	BUF06-	BUF08-	BUF10-				#REC+				
F	LOAC-	BPCLR	CLEAR	CLEAR	CLEAR	CLEAR	CLEAR	CLEAR				#SRSV+				
H	AC00		#SRD0-	#SR02-	#SR04-	#SR06-	#SR08-	#SR10-				#DLST+				
J	AC01	XINT+	BUF00+	BUFD2+	BUF04+	BUF06+	BUF08+	BUF10+				#PAR+				
K	EAC02-	#SRSV-	BAC00	BAC02	BAC04	BAC06	BAC08	BAC10				#EBPC+				
L	EAC03-	#XMT-	BAC00-	BAC02-	BACD4-	BAC06-	BAC08-	BAC10-				#IFMD+				
M	LOAC-		READ	READ	READ	READ	READ	READ				#STRDY				
N	AC02	IOP4	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD				#THRD+				
P	AC03	DEVSLO	BUF01+	BUF03+	BUF05+	BUF07+	BUF09+	BUF11+				#RING				
R	EAC04-	BPCLR	BUF01-	BUF03-	BUF05-	BUF07-	BUF09-	BUF11-				#CARDT				
S	AC05-		#SRD1-	#SR03-	#SR05-	#SR07-	#SR09-	#SR11-								
T	LDAC-	RINT+	BAC01	BAC03	BAC05	BAC07	BAC09	BAC11								
U	AC04	#SRSV-	BAC01-	BAC03-	BAC05-	BAC07-	BAC09-	BAC11-								
V	AC05	#REC-	READ	READ	READ	READ	READ	READ								

	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32
	R123	W002	R111	R001	R111	R107	R202	R123	R123							
A																
B																
C																
D	EAC06-	EAC00	IOP4C	GRPSEL	BMB07-	CTWD3	BT1	BUF0D+	BUF06+							
E	EAC07-	EAC01	CTWD0	DEVND3	BMBD8-	DEVSL3	ADRAC-	BUF01+	BUF07+							
F	LOAC-	EAC02		#REC+	DEVND3	WRITE+	BPCLR	WRITE+	WRITE+							
H	AC06	EAC03	#SRSV+	CLRND	DEVSL3	WRITE-	ADRAC-	AC00	AC06							
J	AC07	EAC04		BBRK+	DEVSL3	BT1	ADRAC+	AC01	AC07							
K	EAC08-	EAC05	BT2A	REDND	IOP1	BT1C	BT1	BUF02+	BUF08+							
L	EAC09-	EAC06	ADRAC+	#REC+	CTWD3	BT2	BKRQ#	BUF03+	BUF09+							
M	LOAC-	EAC07	CLRND	RFDND		BT2A		WRITE+	WRITE+							
N	AC08	EAC08	CLEAR		WRITE-	CLEAR	BT2	AC02	AC08							
P	AC09	EAC09			WRITE-	BPCLRC	BBRK-	AC03	AC09							
R	EAC10-	EAC10	IOP2		IOP4C		BPCLR	BUF04+	BUF10+							
S	EAC11-	EAC11	CTWD3		CTWD3		BBRK-	BUF05+	BUF11+							
T	LOAC-	DIAD11				READ	BBRK-	WRITE+	WRITE+							
U	AC10	DICTL	CLEAR		LOAD	BT1C	BT2	AC04	AC10							
V	AC11				LOAD	REDND	ADRAC-	AC05	AC11							

TABLE III-6.

PANEL 2 ... PORT O/LINE ADAPTOR # (WITHOUT DATA BREAK)

	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16	
	W201C	EIAR	R111	W501	R111	R001	R302	R111	R201	R205	R205	R205	R205	R205	R201	R205	
A																	A
B																	B
C		#GND02		#GND04			#GND06									#GND14	C
D	#SOB	#GND02	#RO+	#SRCK	#SDBF+	#REC-		#RECE-		#SHIFT	#SHIFT	#SHIFT	#SHIFT	#SHIFT		#SHIFT	D
E	#ROB	#RINGB	#REC+		#LINE+	#OTNO1	#ROSD+		#SHIFT	#SR01-	#SR03-	#SR05-	#SR07-	#SR09-	#SHIFT	#SDBF+	E
F	#RSB			#SRCK	#OTND1	#REC-	#GND06		#RD+	#ZERSR	#ZERSR	#ZERSR	#ZERSR	#ZERSR	#SR10+		F
H	#CSDB	#RING	#RD-		#OUT1	#OTND2		#REC+		BUF01-	BUF03-	BUF05-	BUF07-	BUF09-		#GND14	H
J	#SRDB	#RING	#RD-		#OUT1	#REC-	#A06JK			#SR01+	#SR03+	#SR05+	#SR07+	#SR09+			J
K	#TROYB	#GND02			#PTBF+	#RSND	#A06JK	#XMTE-	#ZROSR	#SR00-	#SR02-	#SR04-	#SR06-	#SR08-	#ZERSR	#SR11+	K
L	#RINGB	#CSDB		#GND04	#LINE-				#SR00+	#SR00+	#SR02+	#SR04+	#SR06+	#SR08+	#SR11+	#SR11-	L
M	#CDETR	#DELAY		#L04	#OTND2		#BFIX		#SR00-	#MBSR	#MBSR	#MBSR	#MBSR	#MBSR	#SR11-	#FRZE	M
N		#CS+		#L04	#OUT1		#IFMD+	#XMT+		#SHIFT	#SHIFT	#SHIFT	#SHIFT	#SHIFT		#SHIFT	N
P	#SCTB	#CS+					#REC-		#SHIFT	#SR02+	#SR04+	#SR06+	#SR08+	#SR10+	#SHIFT	#PATY+	P
R	#SCRB	#GND02	#RFIX	#SCRB	#XMT-				#RD-	#SR02-	#SR04-	#SR06-	#SR08-	#SR10-	#SR10-	#PATY-	R
S		#SRD3			#XTRO+		#A06ST		#MBSR	BUF02-	BUF04-	BUF06-	BUF08-	BUF10-	#MBSR	#GND14	S
T					#RSND		#A06ST		BUF00-	#SR01-	#SR03-	#SR05-	#SR07-	#SR09-	BUF11-	#EP2	T
U		#STRDY	#DELAY		#RSI					#SR01+	#SR03+	#SR05+	#SR07+	#SR09+		#EP2	U
V		#STRDY			#RSI		#RR1			#MBSR	#MBSR	#MBSR	#MBSR	#MBSR		#ZROSR	V

	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16	
	W602	EIAR		W501	W501	R202	R602	R602	R602	R602	R202	R107	R107	R121	R111	R002	
A																	A
B																	B
C		#GND34		#GND36							#GND43		BKSLB				C
D	#OUT1	#GND34		#SCK	#COTD		#JMP39	#JMP40	#JMP41		#SRSV+	#CAROT	#BRENB	#IOFCS	#ENDI	#SR00-	D
E		#RDB			#COT			#FP3+			#RSYN-	#CDTD	#BR1	#EBPC+	#BRENB	#SR01-	E
F	#SDB			#SCK	#COTD	#PWCLR		#EXMT			#PWCLR	#OY+	BKRQ#	#DTSY+		#DSYND	F
H	#ROSD+	#RDBI				#REC-	#CLOCK	#BRKDN		#CLOCK	#RSYN-	#OY-	#BKRQ+	#F1	#CHRDN	#SR02-	H
J		#RDBI				#REC+	#DTSY-	#ENZR		#SYNC-		#STCK	#ENAX+	#IFMO-	#CHRDN	#SR03+	J
K	#HSB	#GND34			#U37	#SRCK	#ZERSR	#ZROSR	#PWCLR	#START	#SRSV-	#SCK	#ENAX-	#OTSY-	#IFMD-	#DSYND	K
L	#TMRD+	#CDETB		#GND36	#U37	#RECF-	#ZROSR	#START	BPCLR		#REC-	#RD+	#ENBL+	#ESFT	#REC+	#SR04-	L
M				#L36	#L37		#JMP39	#JMP40	#JMP41			#RDBI	#ENBL-	#OY-	#DSYND	#SR05+	M
N	#TROYB	#COT		#L36	#L37						#START	#DTSY+	#END1	#SVC-	#DTSY-	#OSYNO	N
P	#V+B01	#COT					#STCK				#GND43	#DTSY-	#END	#I3PCS	#DTSY-	#SR06+	P
R	#V-B01			#SCTB	#JM37	#PWCLR	#XMT-				#PWCLR	#CS-		#EFRO		#SR07-	R
S	#V+B01				#COT	#XMT-	#SRCK	#CLOCK	#BRKON		#SYNC-	#CS+		#F1		#OSYND	S
T					#JM37	#XMT+	#REC-	#ESFT	#EXMT				#BLOCK	#SVC-			T
U						#STCK	#CLOCK	#SHIFT	#MBSR	#END	#CLOCK		BKSLB	#I3PCS			U
V	#V-B01					#XMT				#FR3+	#SVC-				#ENDI		V

TABLE III-7.

PANEL 2 ... PORT O/LINE ADAPTOR # (WITHOUT DATA BREAK)

	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32	
	R202			R201	·R201	R201	R205	R205	R205	R205	R123	R123		R123			
A																	A
B																	B
C					#GND19	#GND20											C
D	#FR3+						#INVMK	#INVMK	#STCK	#BRKDN	#SRSV+	#EBPC+		#CFR3+			D
E	#DY-			#INVMK	#ADAC	#START			#CLSD-	#RQSO-	#DLST+	#IFMO+		#CFR2+			E
F				BAC07	#GND19	#GND20	#PWCLR	#PWCLR	#PWCLR	#PWCLR	#ENBL+	#ENBL+		#ENAX+			F
H	#LINE-			#REC-				#PAR1		#RS1	EAC00	EAC06		EAC08			H
J	#LINE+			#XMT+			#EJPC+	#PAR+	#CLSD+	#RQSD+	EAC01	EAC07		EAC09			J
K	#CLOCK			#PWCLR	#PWCLR	#PWCLR	BAC05	BAC02	#CS-	#XTRQ-	#PAK+	#STRDY		#CFR1+			K
L	#LINE+			#IFMD+	#BKRQ+		BAC06	BAC02	#CS+	#XTRO+	#RQSD+	#THRO+		#CFRO+			L
M	#FRZE			#IFMD-		#SVC-		#CLOCK		RT1	#ENBL+	#ENBL+		#ENAX+			M
N	#FR3+					#RSTRT	#INVMK	#INVMK	#INVMK	#INVMK	EAC02	EAC08		EAC10			N
P	#PATY-			#INVMK	#FR3+	#REC-	#THRD+	#DLST+	#SRSV+	#XTRQ+	EAC03	EAC09		EAC11			P
R				BAC07	#IFMD-	#XMT+			#SRSV-	#XTRO-	#XTRQ+	#RING		#RQSD-			R
S	#PTBF+			#CLOCK	#START	#XMT-		#SRSV-	#ESRSV		#CLSD+	#CAROT		#RQSD+			S
T				#DTSY-	#XMT-	#REC+	BACTY	BAC01	BAC00	BAC04	#ENBL+	#ENBL+		BKSL#			T
U	#FR3+			#XMT-			BACTY	BAC01	BAC00	BAC04	EAC04	EAC10		DIAD11			U
V	#PATY+			#REC+				#CHRON	#CHRON		EAC05	EAC11		DICTL			V

	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32	
			R301	R111	R121	R121	R121	R001	R111	R603	R602	R205	R205	R205	R205		
A																	A
B																	B
C											#GND59	#GND60	#GND61				C
D			#THRD+	#RQSO+		#EP2		CTWD1		IOP4	#JMP59	#CLOCK	#FR1+	#LDAUX	#LDAUX		D
E			#XMTND	#CLSD+		#RD+		#BLND		#ENBL-				#CFRO-	#CFR2-		E
F			#CAROT	#XMTND		#DTSY+		#BLOCK	#BLND	#INVMK		#FRZE	#FRZE	#PWCLR	#PWCLR		F
H			#XMTND	#XMTE-	#ENZR	#EP2	#ADAC	#BLND	#ENBL-		#SVC-	#CFRO-	#CFR2-				H
J			#STRDY	#XMTE-	#REC+	#SR11+	ADRAC+	CTWD2	#ENBL-		#GND59	#FRO+	#FR2+	#CFR3+	#CFR2+		J
K			#XMTND	#FR3+	#IFMD+	#XMT+	BKSL#	#AXND		#ZROSR	#FRZE	#EFRD	#GND61	BAC11	BAC09		K
L			#FR2+	#FRD+	#EXMT	#EP2	#BRKDN	#BLOCK		#XTRQ+	#PWCLR	#EFRD	#GND61	BAC11	BAC09		L
M			#DYND	#DYND	#IFMD+	#RD+	BKSL#	#AXND	#AXNO	#LOFR	#JMP59	#LOFR	#LOFR				M
N			#FR1+	#DY-	#XTRQ+	#REC+	BBRK+	#REC+	#ENAX-			#FRO+	#FR2+	#LDAUX	#LDAUX		N
P			#DYND	#DY-	#XMT+	#IFMD+	BT1C	#PARND	#ENAX-	#MBSR	#IFMD-	#FR1+	#FR3+	#CFR1+	#CFR3+		P
R			#EBPC+	#REC+	#RECE-	#ESRSV	#PAR1	#DY+	#RD+	IOP4	#XMT-			#CFR1-	#CFR3-		R
S			#DYND	#IFMD+	#RCSD-	#XMT+	#RD-	#PARND	#PATY-	#ENAX-	#IFMD+	#CFR1-	#CFR3-				S
T			#IFMO+		#CLSD-	#XTRQ+	#REC+		#PARNO	#LDAUX	#REC-	#GND60	#GND61	BAC10	BAC08		T
U			#DYND	#ESRSV	#CAROT	#IFMD+	#DY+		#PAR1		#RSTRT	#GND60	#GND61	BAC10	BAC08		U
V					#STRDY		#PATY+					#LOFR	#LOFR				V

TABLE III-8.

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3. REPORT TITLE

A 201A DATA COMMUNICATION ADAPTOR FOR THE PDP-8: PRELIMINARY ENGINEERING DESIGN REPORT

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)
Technical Report

5. AUTHOR(S) (Last name, first name, initial)

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13. ABSTRACT

This report discusses the design and use of equipment built for data communication to and from a PDP-8 through a 201A data set. The purpose of the data communication interface is to allow a PDP-8 to send and receive digital data through a 201A data set in half-duplex mode. Basic design objectives and decisions are described first. A brief overall system description together with a sketch of a data format scheme and programming considerations is followed by a detailed description of the interface logic.

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14. KEY WORDS	LINK A ROLE	LINK A WT	LINK B ROLE	LINK B WT	LINK C ROLE	LINK C WT
Data Communication						
Logical Design						
Data Transmission						
Serial Synchronous Data Transmission						
Digital Computer Interface						

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